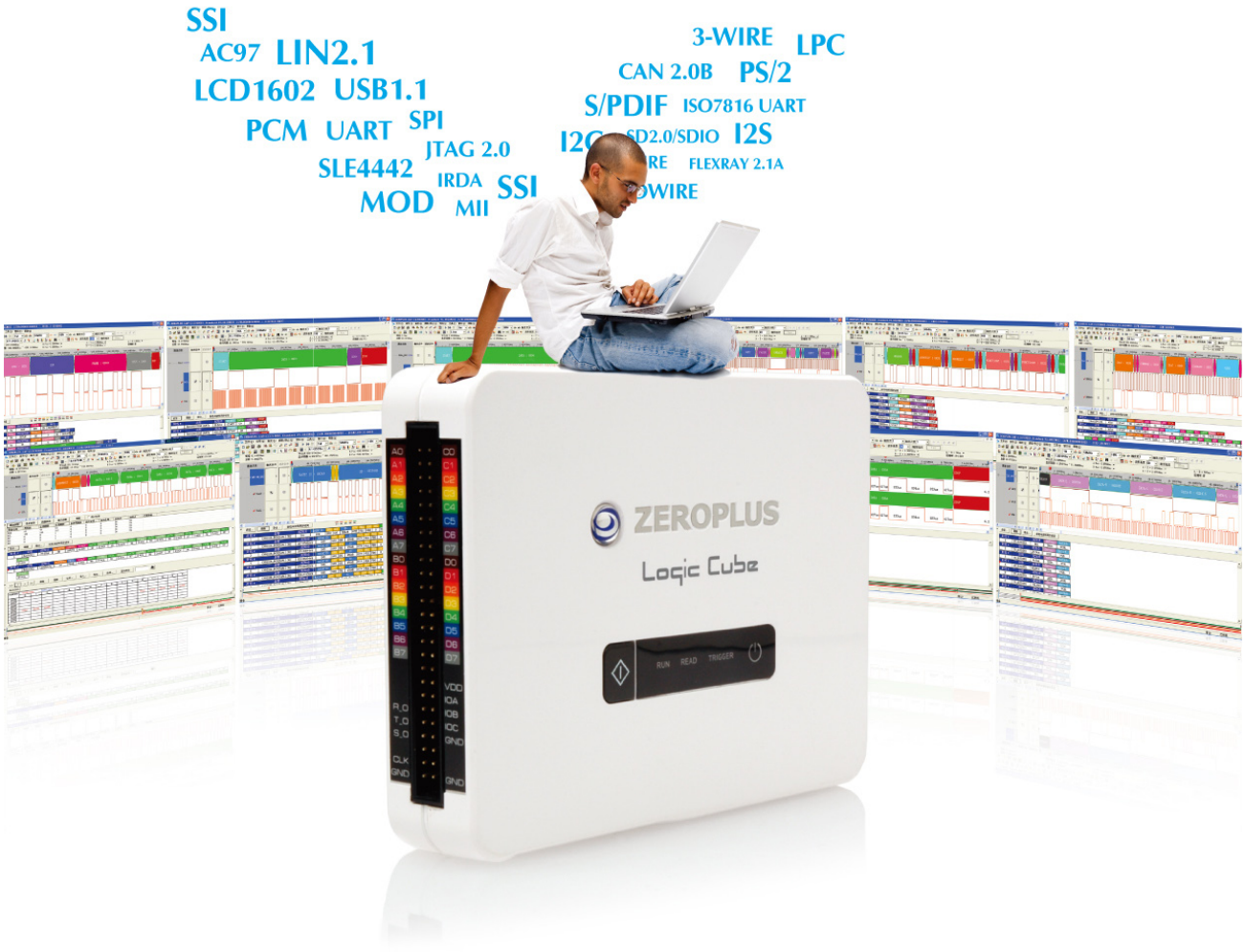
# Data Filtering and Edge Storage Functions

## Analysis and Debugging with Logic Analyzer – Fast, Fierce, Accurate

## Purpose Discussion

As the digital technology era has arrived in recent years, there has been explosive growth for various 3C products, resulting in continual advancement of digital signal processing technology. Various types of digital communication protocols have been continually released, especially by large manufacturers as they need to grasp new technologies and lead technology trends. They continually released new specifications for digital communications; however, these digital communication technologies present technology developers problems. In order to break through this dilemma, logic analyzers, which are specifically for analyzing digital signals and communication protocols and also these types of digital signal communication data, provide various practical analysis functions and further process complicated digital signals.

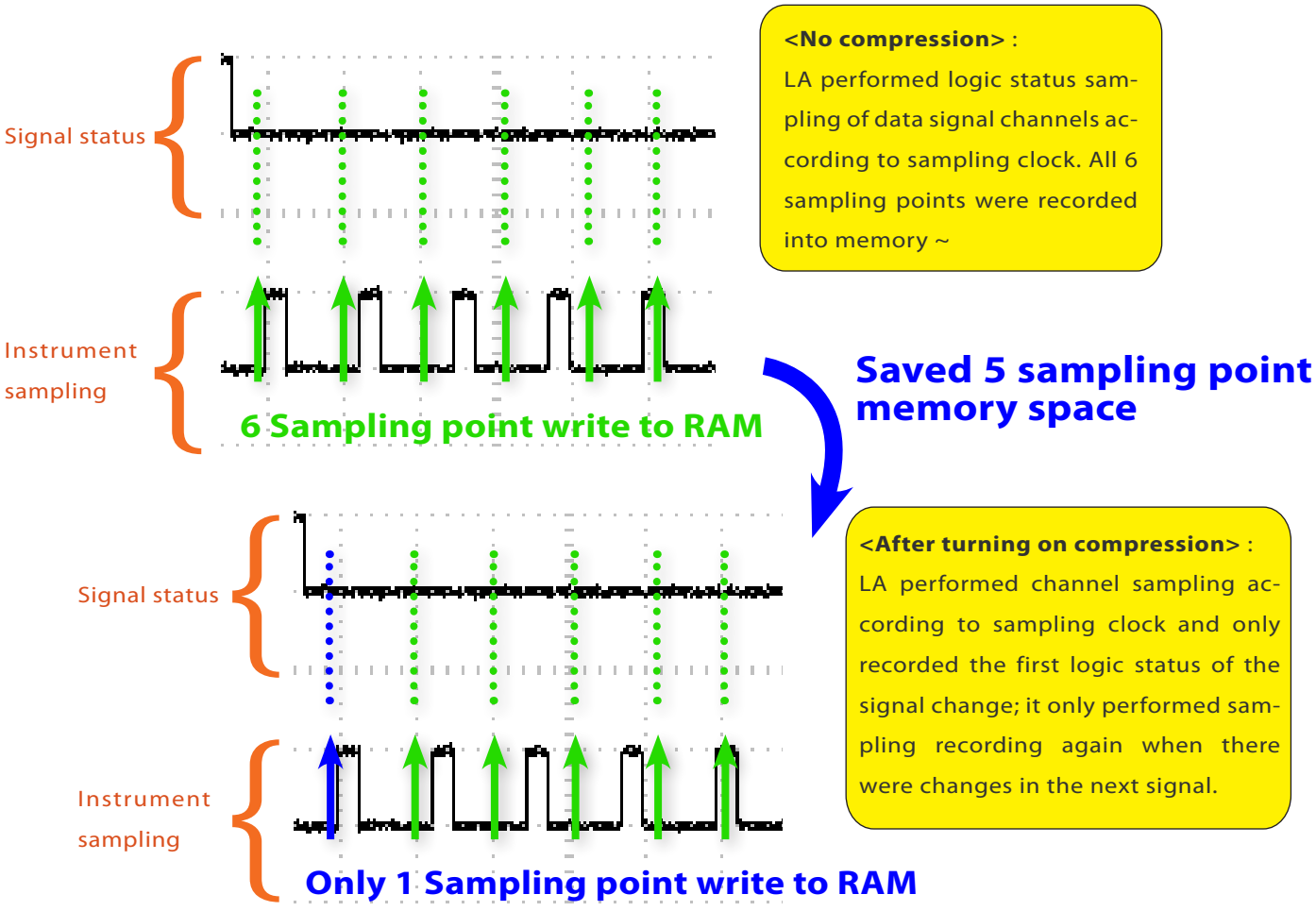


# Exert maximum benefit of limited memory by using compression functions

Frequently seen basic architecture, including UART, SPI, I2C and CAN bus etc., has a simple communication architecture and wide application range. But when issues occur, the user will need to track and analyze a lot of device signals, which most of the time are difficult to resolve because there is insufficient memory depth for the measuring instrument. This is when compression functions may be used to exert maximum benefit of the instrument's memory.

Compression function is an HW compression technology that processes signals at the instrument's input terminal, and determines the status of every received signal, and then only retains the signal's edge change status data for data storage (Figure 1). There are four basic statuses for digital signals, which are high, low, rising edge and falling edge.

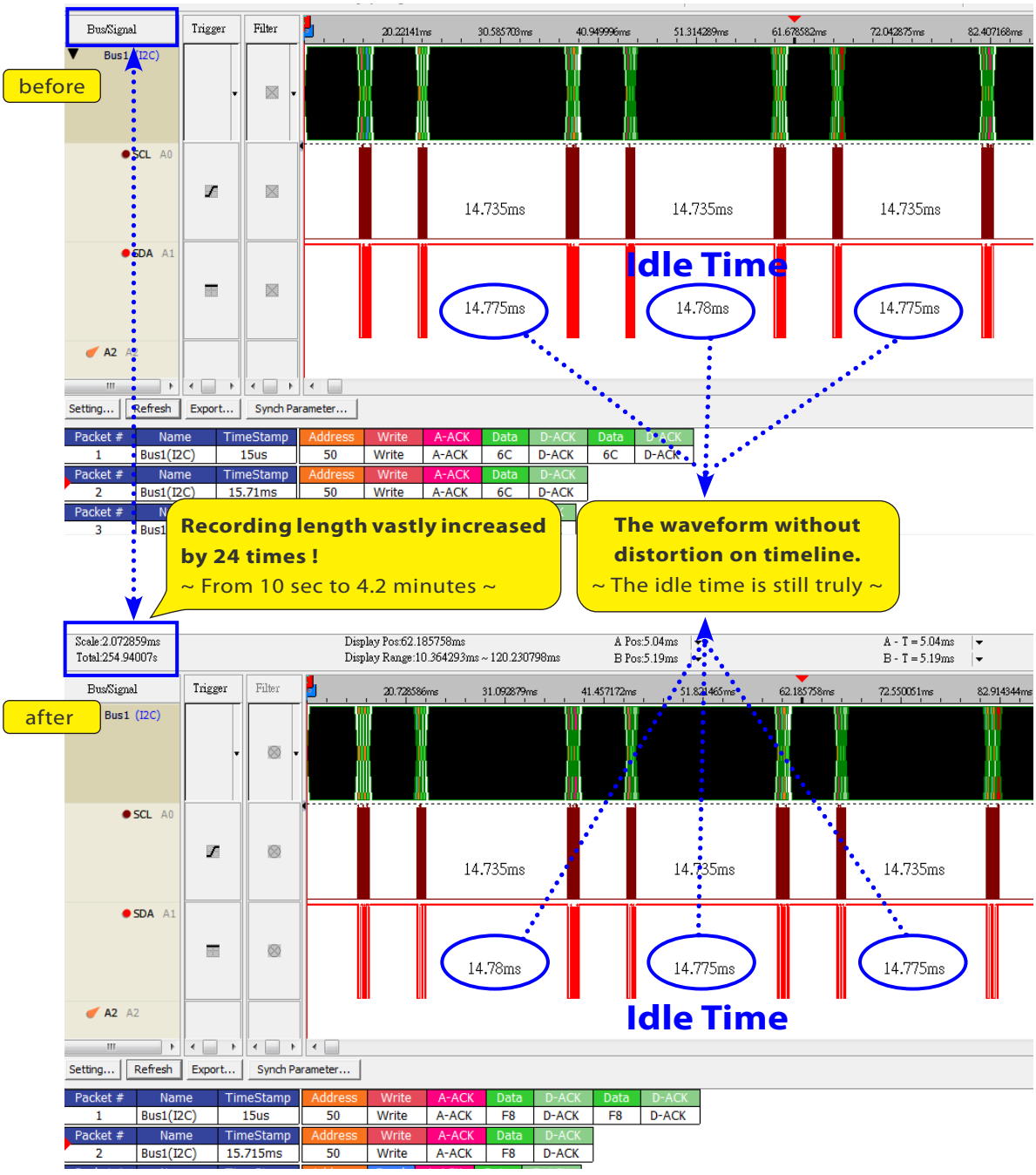
When the memory is filled with data, the logic analyzer will send the data back to the computer terminal, so the user does not have to worry about the data timeline being distorted after the data has passed through the HW compression technology. When the data is sent back to the computer terminal, the software will perform a "software unpack for the data timeline"; this is the compression technology concept of ZEROPLUS TECHNOLOGY HW compression software unpack.




▲ Figure 1: Edge storage difference before and after turning on compression function.

## Effectively use compression technology to avoid device idle time in order to achieve maximum depth memory utilization

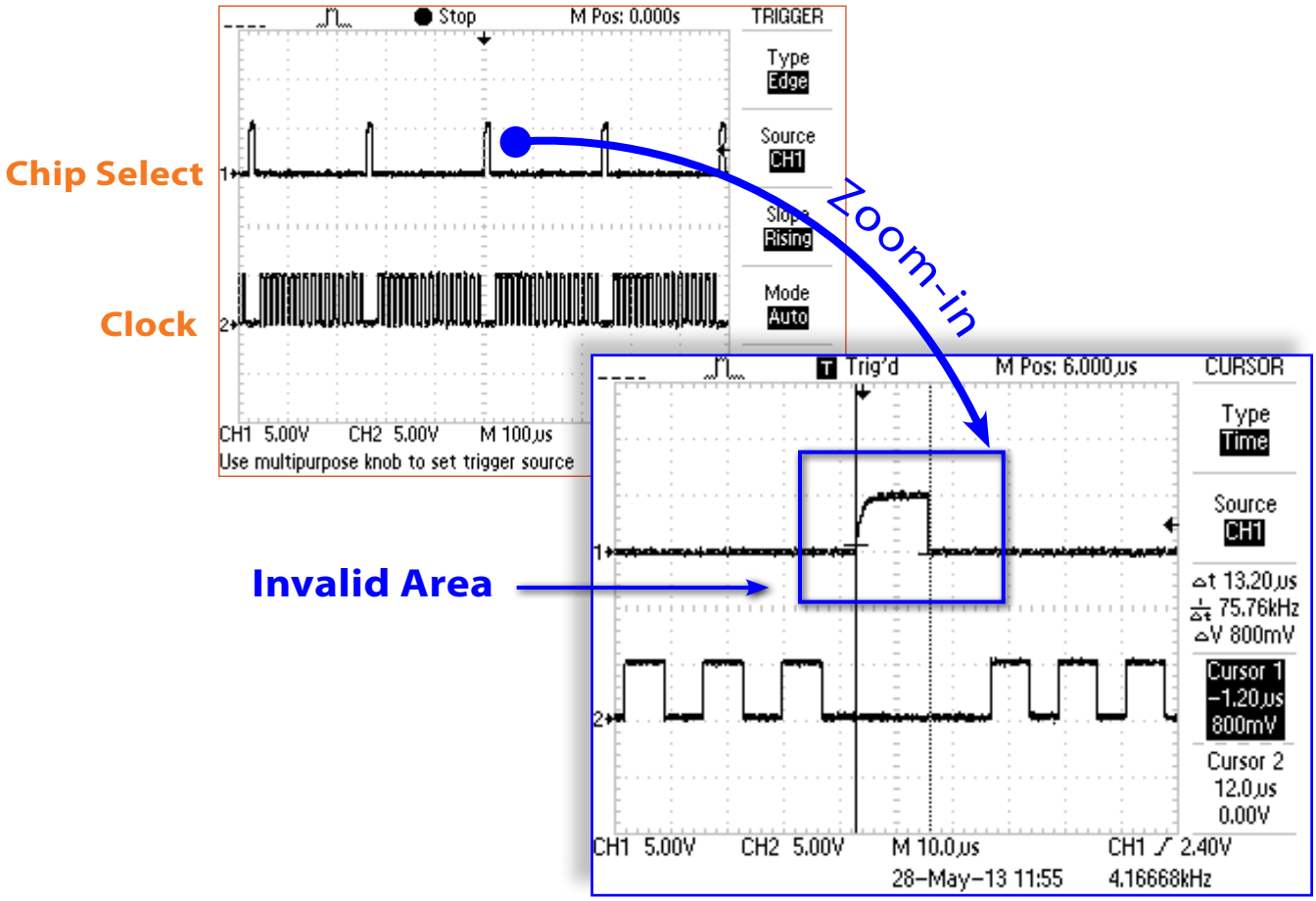
Using the most commonly used I2C bus in current electronic products as an example, the basic communication 2 pin only requires lines to perform communication, and this communication protocol is mostly used on the control and communication between multiple "microprocessors (MCU)", especially EEPROM data access applications. However, because of the write configuration analysis of multiple MCU and registers, the idle time is usually long and results in the inability to capture the data that we want to analyze, and increases the difficulty in I2C bus debugging. This is when the compression function can be used to increase the length of signal recording, as shown in Figure 2 below.




▲ Figure 2: Actual comparative testing of the ZEROPLUS Logic Analyzer (before and after compression)

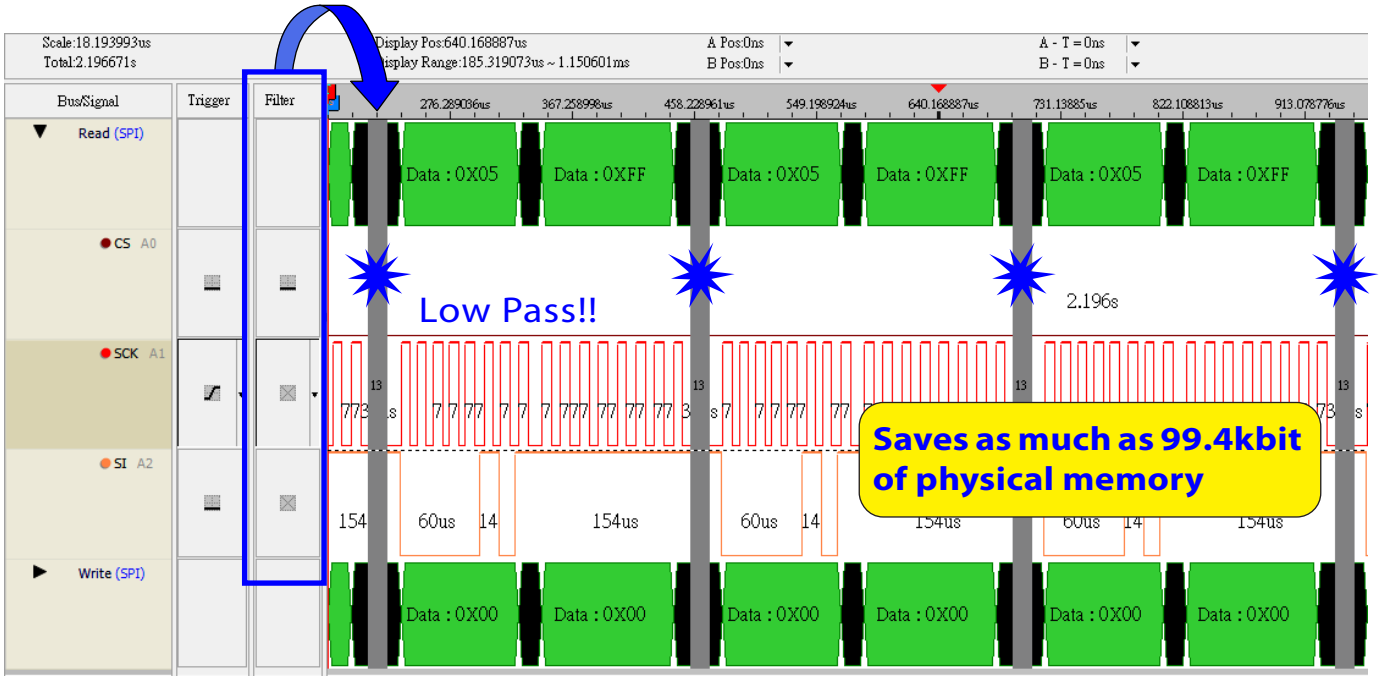
## Use the filtering function to filter valid data and analyze only what you want to see!

SPI bus is another frequently seen commonly used communication protocol in electronic products; its specification uses 4 pins to perform communication; 1 clock pin, 1-in/1-out single channel data transmission pin, and the final pin is chip select (CS). The CS pin is mainly used to determine whether there is data that needs to be transmitted to the enable pin, and uses active low to represent starting transmission of valid data (as shown in Figure 3) .




▲ Figure 3: SPI bus signal active low

When analyzing SPI communication protocol, most of the time engineers only want to analyze valid data where the CS pin is low and do not want to see other signals. This is when the filtering function can be used to help engineers filter data effectively and easily, as shown in Figure 4 below.




▲ Figure 4: The filter function of the logic analyzer can easily filter out unnecessary data

# Conclusion

ZEROPLUS TECHNOLOGY has accumulated over 7 years of practice experience and technical capabilities in manufacturing logic analyzers; we do everything on our own from R&D to manufacturing, so we have deep understanding of the engineer's hard work and difficulties in analyzing digital signals. Integration with software and hardware not only supports decoding of hundreds of digital communication protocols, the hardware functions also continually advances with time. Through the two hardware technologies compression and filtering, we hope to provide engineers with more flexible usage space in order to satisfy the customer's usage needs, and further achieve resolving of all bug problems. ZEROPLUS TECHNOLOGY provides professional technical personnel to satisfy customer needs and provide technical support; we believe we are the best choice for you.

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