Measurement and Analysis Introduction of Protocol Microchip UNI/O

Brief Introduction

In times of the booming information, the 3C products which are used in our lives are constantly evolving. For example, the early mobilephone is very bulky and the standby time is so short; with the help of the different Protocol Analyzers, the parts in the products will be evolved, which make the volume of the mobilephone become small and the function become strong. Certainly, the EEPROM is being developed toward this direction. Most of the Read/Write Controls of the traditional EEPROM are transmitted by the SPI or I2C. But if the SPI is used as a transmission interface, the IC Pins to be used need four signal channels (SCK, CS, MOSI, MISO). What's more, if the I2C is used as a transmission interface, it will also need two signal channels (SCK, SDA). The UNI/O, which is developed by the Microchip Technology, is a kind of one-line Control Interface. That is to say, it only needs one signal channel to realize the EEPROM Read/Write actions. The volume of the Memory Components of the UNI/O is small, but it owns more functions, such as Status Register, Software Write Protection for ¼, ½ or Full Array, Noise Filter and Effective ESD Protection, which is used to make sure that the components work normally.

UNI/O

The UNI/O is a kind of the Asynchronous Protocol Analyzer, which is designed for the Low-speed communication part in the Embedded System by the Microchip Technology. The UNI/O only requires one signal channel (SCIO) to transmit the data between the Master Device and Slave Device.

For the data encoding, the UNI/O uses the Manchester encoding. It can judge the Logic status of the Bit according to the change in a Bit Period. See the below figure 1:

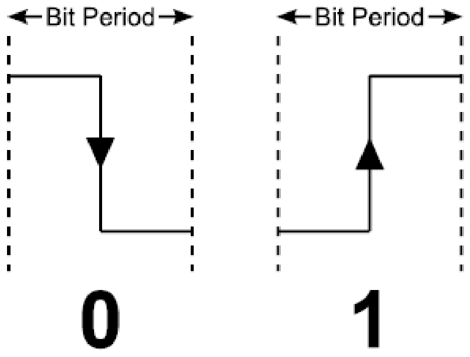
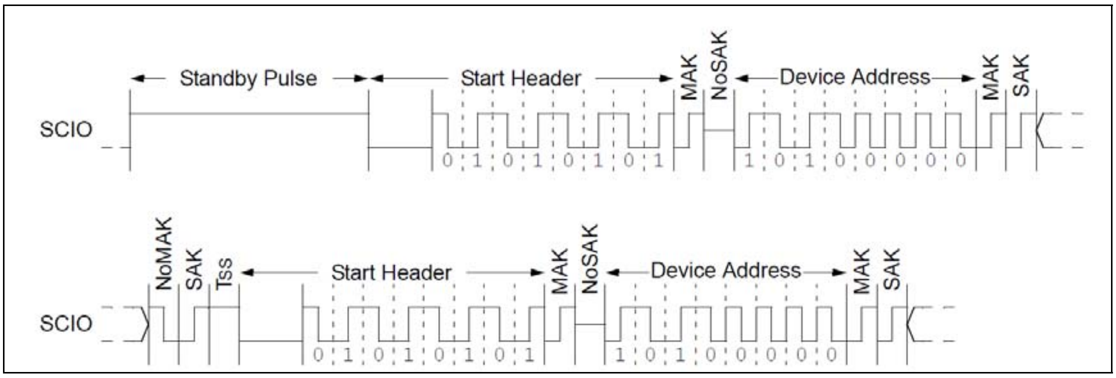


Figure 1: UNI/O Bit Period

Data Structure

A segment of the UNI/O signal consists of several packets, including Standby Pulse, Start Header, Device Address（Family Code, Device Code）, Acknowledge Sequence, Command and Data.



Standby Pulse: It makes the UNI/O enter the standby status, which will appear in front of the Start Header packet. It is the signal of the Logic 1 continuously, the time of the signal can keep 600us at least.

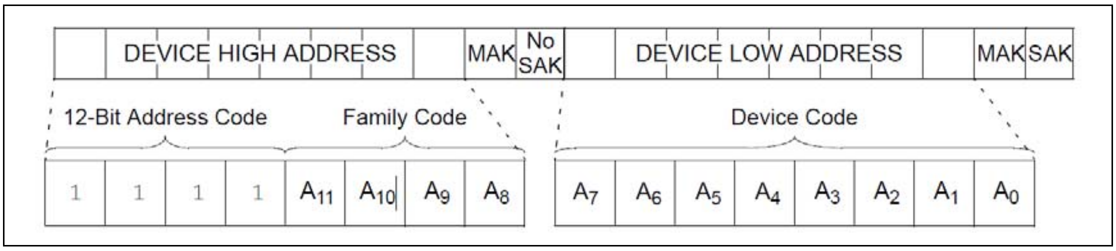
Start Header: It is defined as a special Byte in the UNI/O specification, the purpose is that it is used for making the Clocks between the Master End and Slave End synchronous. The Start Header begins at the cut-off point between the signal of Logic 0 and the Standby Pulse, its data is 0x55. After the Start Header Byte is transmitted, a group of ACKs are also to be transmitted for Acknowledge, which consist of the MAK (NoMAK) and the SAK (NoSAK) fixedly.

Acknowledge Sequence: After a Byte is transmitted for each time, the 2-bit ACK will also be transmitted. The first Bit is the MAK (Master Acknowledge), and the second Bit is the SAK (Slave Acknowledge).

When the MAK (Master Acknowledge) Bit is “1”, it denotes that there is the response for the Master Device, and the data will be transmitted continuously at this moment. When the MAK Bit is “0”, there is no response (use the NoMAK/No Master Acknowledge to denote), which denotes that the transmission of the data has been finished.

SAK (NoSAK): It is the ACK signal transmitted by the Slave. When the SAK is transmitted by the Slave, the value of the Bit is “1” and the value of the NoSAK is “0”. When the response can’t be confirm from which the Slave is or there is not the response from the Slave, this Bit is in the uncertain status; so the NoSAK following the Start Header is in the uncertain status.

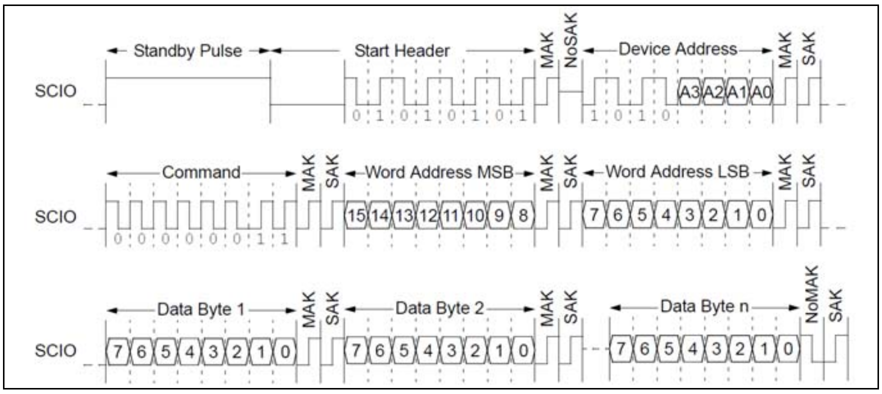
Device Address: It appears in back of the Start Header, which consists of the Family Code and the Device Code. It can be divided into 8-Bit Address and 12-Bit Address, which is used to decide that the Master Device starts transmitting with which Slave Device. The format of the Device Address is decided by the high four bits in the Device Address. When all the values of the high four bits in the Device Address are “1”, the format of the Device Address is the 12-Bit Device Address mode.,To the contrary, it is the 8-Bit Device Address mode. The Device Address in the 12-Bit Device Address consists of 2 Bytes. The high four bits of the first Byte are fixed as “1”, and the low four bits are the Family Code, and the second Byte is the Device Code. When the Device Address in the 8-Bit Device Address consists of one Byte, the high four bits of the first Byte are Family Code, and the low four bits are Device Code


DEVICE HIGH ADDRESS
MAK
No SAK
DEVICE LOW ADDRESS
MAK
SAK
12-Bit Address Code
Family Code
Device Code
1
1
1
1
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0

Family Code: The four bits in the Device Address are used to denote the status of the current communication Device, such as the Memory, Temperature Inductor and A/D Converter.

Device Code: Both of the Device Code and the Family Code are included in the Device Address, the Device Code can be divided into 4-Bit or 8-Bit according to the different formats of the Device Address. It is mainly used to distinguish the Device with the same Family Code. If the Device Address is the 8-Bit Address, the Device Code has 4 bits; if the Device Address is the 12-Bit Address, the Device Code has 8 bits.

Command: When the Master Device confirms the Slave Device to be transmitted, it will transmit a Byte to represent the type of the performed action; there are nine kinds of the different Commands in total. When the Command is transmitted, the transmission starts from MSB. Table 1 is the Command List.


Standby Pulse
Start Header
MAK
NoSAK
Device Address
MAK
SAK
SCIO
0 1 0 1 0 1 0 1
1 0 1 0
A3 A2 A1 A0
Command
MAK
SAK
Word Address MSB
MAK
SAK
Word Address LSB
MAK
SAK
SCIO
0 0 0 0 0 0 1 1
15 14 13 12 11 10 9 8
7 6 5 4 3 2 1 0
Data Byte 1
MAK
SAK
Data Byte 2
MAK
SAK
Data Byte n
NoMAK
SAK
SCIO
7 6 5 4 3 2 1 0

Command Name	Command Code	Hexidecimal Code	Description
READ	0000 0011	0X03	Read the data from the appointed Address of the Memory Array.
CRRD	0000 0110	0X06	Read the data from the current Address of the Memory Array.
WRITE	0110 1100	0X6C	Write the data in the appointed Address of the Memory Array.
WREN	1001 0110	0X96	Write Enable.
WRDI	1001 0001	0X91	Write Disable.
RDSR	0000 0101	0X05	Read the data from the Status Register.
WRSR	0110 1110	0X6E	Write the data in the Status Register.
ERAL	0110 1100	0X6D	Clear the data in the Array to 0X00.
SETAL	0110 0111	0X67	Write the data in the Array as 0XFF.

Table 1: UNI/O Command List

Actual Measurement of UNI/O Signal

Zeroplus Technology Logic Analyzer can support the decoding of UNI/O Signal. In this example, we use the SDK of the MPLAB Starter Kit for Serial Memory Products（Part Number: DV243003）of the Microchip to do measurement, the attached EEPROM 11LC160 in the SDK to read and write the data and the Protocol Analyzer UNI/O of Zeroplus Technology to decode the data.

11LC160 is a kind of the EEPROM with 16K RAM Size, the Figure 2 is the Pin Description of the 11LC160.

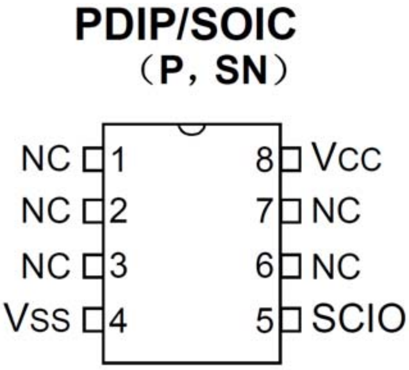


Figure 2: 11LC160 Pin Description

The fifth Pin of 11LC160 is the SCIO known by the above Pin Description, so it is necessary to connect the SCIO to Logic Analyzer when performing the measurement

Next, set the measurement environment: Connect the A0 and GND on the Logic Analyzer to the SDI/SDA and GND on the MPLAB Starter Kit for Serial Memory Products respectively through the attached Test Probe. When the connection is finished, see the Figure 3 as below.

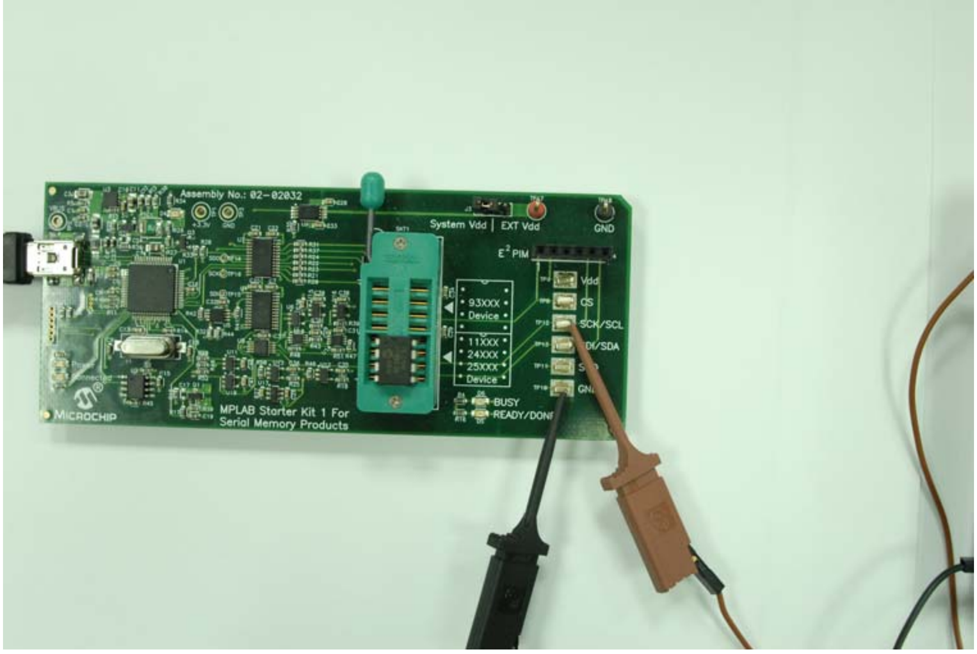
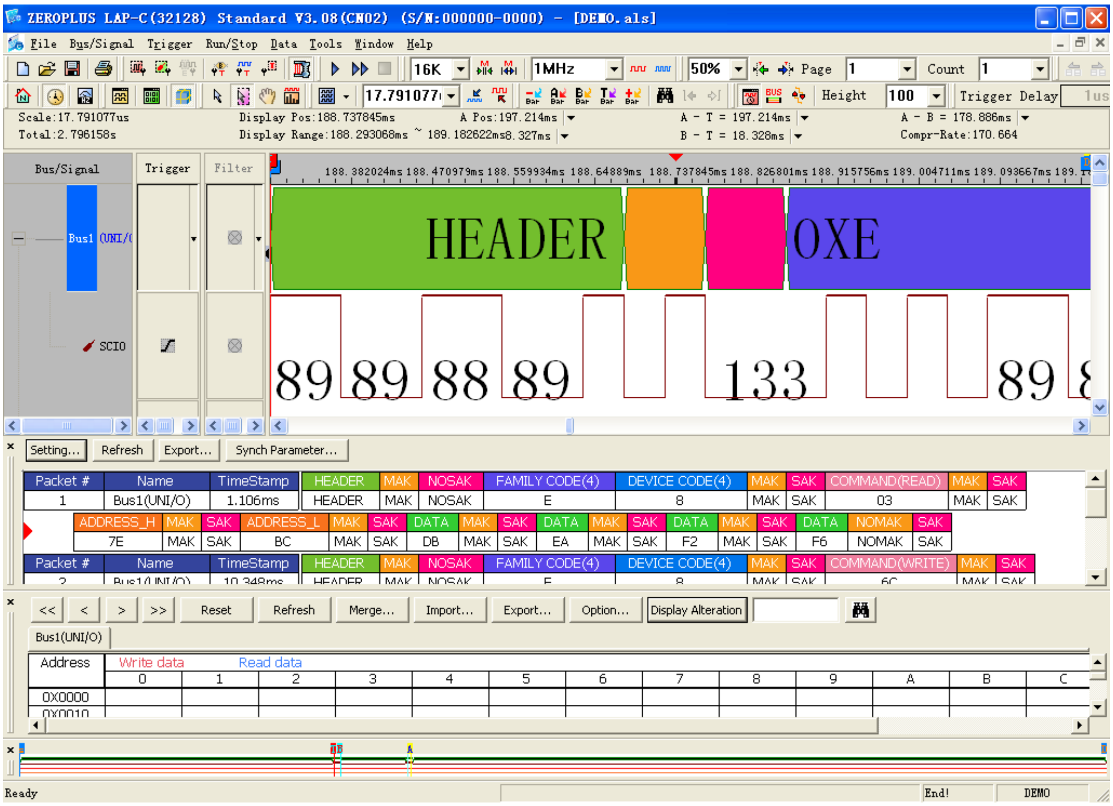

Assembly No.: 02-02032
System Vdd
EXT Vdd
GND
E² PIM
Vdd
CS
SCK/SCL
SDI/SDA
93XXX Device
11XXX 24XXX 25XXX Device
BUSY
READY/DONE
MICROCHIP
MPLAB Starter Kit 1 For Serial Memory Products

Figure 3: Connection Completion of Measurement Environment

When the connection is completed, the Zeroplus Logic Analyzer Software can be activated to measure the signal (Please refer to Zeroplus Technology website, www.zeroplus.com.tw, to learn the operating instructions of Logic Analyzer); the captured waveform image is displayed as below (Refer to Figure 4).


ZEROPLUS LAP-C(32128) Standard V3.08(CN02) (S/N:000000-0000) - [DEMO.als]
File Bus/Signal Trigger Run/Stop Data Tools Window Help
16K
1MHz
50%
Page 1
Count 1
17.791077
Height 100
Trigger Delay
Bus/Signal
Trigger
Filter
Bus1 (UNI/O)
SCIO
HEADER
0XE
89 89 88 89 133 89
Setting... Refresh Export... Synch Parameter...
<< < > >> Reset Refresh Merge... Import... Export... Option... Display Alteration
Bus1(UNI/O)
Address Write data Read data
0 1 2 3 4 5 6 7 8 9 A B C
0X0000
0X0010
Ready
End!
DEMO

Scale:17.791077us
Total:2.796158s
Display Pos:188.737845ms
Display Range:188.293068ms ~ 189.182622ms8.327ms
A Pos:197.214ms
A - T = 197.214ms
B - T = 18.328ms
A - B = 178.886ms
Compr-Rate:170.664

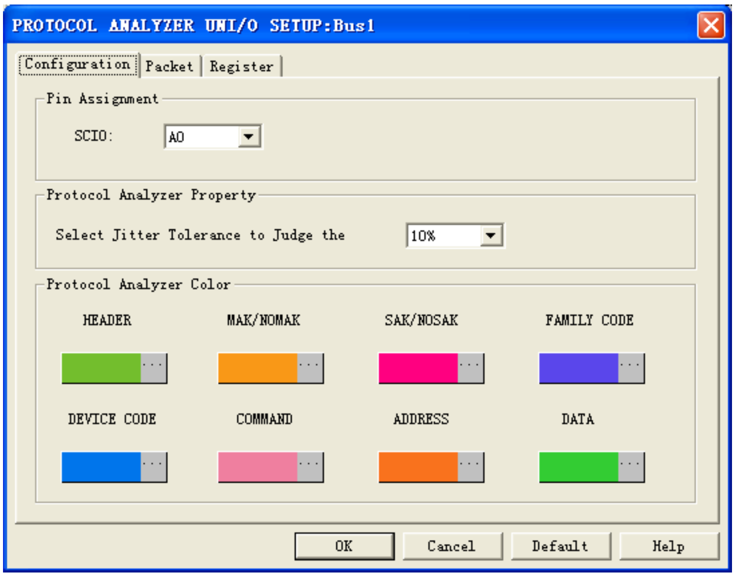
Packet #	Name	TimeStamp	HEADER	MAK	NOSAK	FAMILY CODE(4)	DEVICE CODE(4)	MAK	SAK	COMMAND(READ)	MAK	SAK
1	Bus1(UNI/O)	1.106ms	HEADER	MAK	NOSAK	E	8	MAK	SAK	03	MAK	SAK

ADDRESS_H	MAK	SAK	ADDRESS_L	MAK	SAK	DATA	MAK	SAK	DATA	MAK	SAK	DATA	MAK	SAK	DATA	NOMAK	SAK
7E	MAK	SAK	BC	MAK	SAK	DB	MAK	SAK	EA	MAK	SAK	F2	MAK	SAK	F6	NOMAK	SAK

Packet #	Name	TimeStamp	HEADER	MAK	NOSAK	FAMILY CODE(4)	DEVICE CODE(4)	MAK	SAK	COMMAND(WRITE)	MAK	SAK
2	Bus1(UNI/O)	10.348ms	HEADER	MAK	NOSAK	E	8	MAK	SAK	6C	MAK	SAK

Figure 4: Captured UNI/O Signal Waveform

The Protocol Analyzer UNI/O of Zeroplus Technology Logic Analyzer not only can analyze the packet of signal automatically, but also can set the Jitter Tolerance automatically according to the data of the signal.


PROTOCOL ANALYZER UNI/O SETUP:Bus1
Configuration
Packet
Register
Protocol Analyzer Color
HEADER
MAK/NOMAK
SAK/NOSAK
FAMILY CODE
DEVICE CODE
COMMAND
ADDRESS
DATA
OK
Cancel
Default
Help

Pin Assignment
SCIO: A0

Protocol Analyzer Property
Select Jitter Tolerance to Judge the 10%

Figure 5: Protocol Analyzer UNI/O Setup Dialog Box

Selelct Jitter Tolerance to Judge the: Set the Change Edge Offset Range of the Decoding in the Bit Period Decoding of the Manchester Encoding, the default is 10%, which indicate that the Change Edge can be judged in the range (40%~60%) of the Bit Period. There are three options (5%, 10%, 15%) from the pull-down menu for users to select.

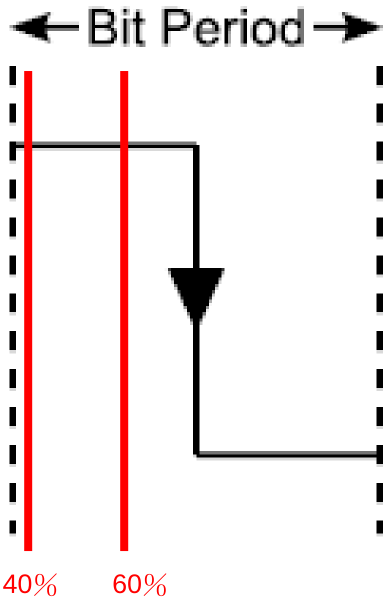


Figure 6: Jitter Tolerance Diagram

Conclusion

With the trend of the volume zoom-out of the Consumer Electronics, the circuit elements in the products should be developed corresponding to this tide. The Protocol Analyzer UNI/O which is developed by the Microchip is a good example. When we use the EEPROM to do the tranmission formerly, most of us will use the I2C or SPI; but both of them need occupying a lot of IC Pins, so there is no way to shorten the volume of the circuit. For the Protocol Analyzer UNI/O, it only needs one Pin, SCIO, to achieve the purpose of Data Transmission, which can make more Electronic Products own the smaller volume and the stronger function.

"When the Small-size Micro-controllers and Storage Devices are attracted by the people's attentions gradually, the UNI/O Series is another choice for users, which offers the miniaturized and low cost advantage to engineers and makes the customers design the circuit and develop hardware more easily." Said Alex Martinez, the Product Marketing Manager of Microchip Memory Department,.

Zeroplus Logic Analyzer can support more than seventy Protocol Analyzer Modules at present. When the R&D engineers analyze the Protocol Analyzer signal, they can shorten the time of project development according to the automatic decoding of the software and make the product on the market earlier. There is no need to decode the signal to be analyzed by manual when facing different digital signals. If you want to know more detailed information, please visit our website, www.zeroplus.com.tw.

Conference：
http://techtrain.microchip.com/webseminars/ArchivedDetail.aspx?Active=160
http://en.wikipedia.org/wiki/UNI/O
http://www.microchip.com/stellent/idcplg?IdcService=SS_GET_PAGE&nodeId=2542&param=en535312