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Measurement and Analysis Introduction of Protocol Analyzer PCI

Whether in the Industrial Computer or PC, the CPU plays an important role. It is similar to the brain of people, which deals with much information which is from the peripheral or sends out information. However, only the CPU can't compose a computer system. It needs different interfaces to connect with the peripheral devices so that a computer can start operating. The PCI is just that kind of Protocol Analyzer.

The PCI is originally developed to fulfill the 486 Series and Pentium Series Processor. It has become the common interface in the current computer system. It has superseded the early ISA and VESA to become the mainstream, too. With the development of the technology, some interfaces with quicker speed have been developed from PCI, such as PCI-X, PCI-Express and so on. Although the PCI-Express has gained a main place in PC systems, the PCI also has earned a place in the Industrial Computer or Embedded System.

The standard of PCI has been developed by Intel in 1990. Intel issued the PCI1.0 in 1992. The PCI didn't become the standard for communicating between the motherboard and the peripheral interface until the PCI-SIG (PCI Special Interest Group) issued the PCI2.0 in April, 1993.

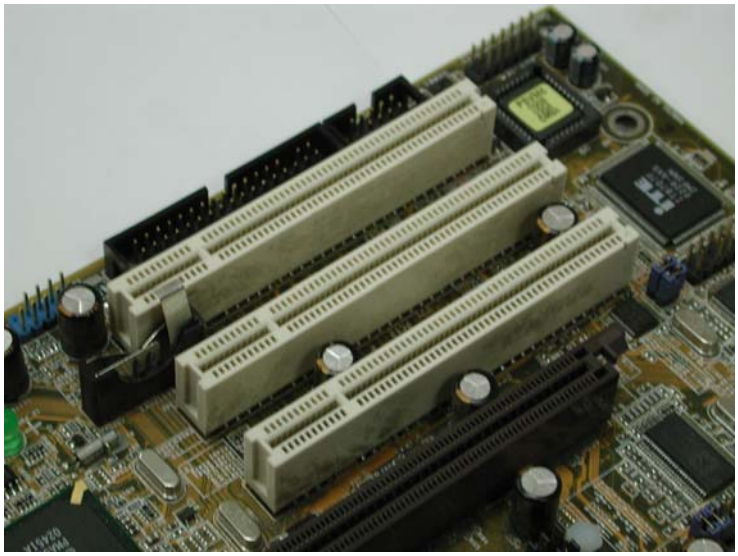

Figure 1: PCI Slot on the Motherboard

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Development History of the PCI Version:

- **PCI1.0 (1992):** It is a 32Bits parallel synchronous Protocol Analyzer; the Clock Frequency is 33MHz; the most quantity of data transmission is 132Mbps.

- **PCI2.0 (1993):** It redefines the specifications of the Expansion Slot and Interface Card, and the power supply is 5V and 3.3V.

- **PCI2.1 (1995):** It adds 66MHz Clock Frequency. The power supply only needs 3.3V when using the 66MHz. The most quantity of data transmission is 264Mbps in 32Bits, 66MHz Clock Frequency; the most quantity of data transmission can reach 528Mbps in 64Bits, 66MHz Clock Frequency.

- **PCI2.2 (1998):**It increases a new Interrupt Mechanism which is the MSI (Message Signaled Interrupts).

- **PCI2.3 (2002):** The 2.3 Version is the mainstream version, which is widely used at present. The use of power supply is 3.3V but not 5V. It adds the specifications of Short Card and the SM Bus.

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The Special Chip for the Protocol Analyzer PCI

The Protocol Analyzer PCI is very complex. It is normal to use the editable Logic Chip to complete the Protocol Analyzer PCI when developing the product about PCI Interface, but the complexity and difficulty are prodigious. In order to simplify the design, users can use the Protocol Analyzer PCI Chip which is produced by the third party, such as the PCI9080, PCI9052, PCI9060ES of PLX, the S5933, S5920 of AMCC, and the i960RP of Intel, and so on.

- PCI (Peripheral Component Interconnect) is mainly used for communicating with the external devices in the computer's motherboard. The standardized PCI can be divided into two types:
  1. An Integrated Circuit which is embedded in the motherboard directly. It is called Planar Device in the PCI specifications.
  2. An Expansion Card which is installed in a slot.

Moreover, the Protocol Analyzer PCI uses the DMA (Direct Memory Access) Mode to transmit data when it controls the peripheral devices. And the usage rate of CPU is lower; it can improve the system efficiency greatly.
According to the directivity and the drive characteristics of the Data Transmission, the PCI can be divided into five types:

- **in:** Input the signal.
- **out:** Output the drive signal.
- **t/s:** It denotes the bidirectional Tri-State Input/ Drive Signal Output.
- **s/t/s**：（Sustained Tri-State）
- **s/t/s:** It denotes the Sustained Tri-State.
- **o/d:** It denotes the Open Drain.

The number of the Signal Channel of Protocol Analyzer PCI is 100 in total; the following is the

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specific explanation:

1.System Signal		
Signal Name	**State Type**	**Description**
CLK	in	Supply the Clock Signal for all the channels of PCI; the highest Clock Frequency can reach 66MHz.
RST	in	It is the Reset Signal. It can reset the relative signals of the working storage or the timing register of the PCI.
2. Address and Data Line		
Signal Name	**State Type**	**Description**
AD0~AD31	t/s	It is the shared Input Signal and Output Signal for the Address and Data.
C/BE0~3	t/s	It is the shared Input Signal and Output Signal for Command and Bit.
3. Control Signal		
Signal Name	**State Type**	**Description**
FRAME	s/t/s	It is the Frame Period Signal.
IRDY	s/t/s	The Master Device is ready to start exchanging data.
TRDY	s/t/s	The Slave Device is ready to start exchanging data.
STOP	s/t/s	The signal is used to stop the Data Transmission. It is sent from the Slave Device to the Master Device to end the Data Transmission.
LOCK	s/t/s	It is the Lock Device. It is used to fix the Bus Device to make sure the Data is correct during the transmission.
IDSEL	s/t/s	It is the Initialization Device.
4. Arbitration Signal		
Signal Name	**State Type**	**Description**
REQ	t/s	It is the Request for the Data Transmission of the Protocol Analyzer.
GNT	t/s	It is the Grant for the Data Transmission of the Protocol Analyzer.

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5. Error Report Signal		
Signal Name	**State Type**	**Description**
PERR	s/t/s	It is the Parity Error Report.
SERR	o/d	It is the System Error Report.

6. Interruption Signal		
Signal Name	**State Type**	**Description**
INTA ~ INTD	o/d	It is used for the Function Interruption.
7. Cache Support Signal		
Signal Name	**State Type**	**Description**
SBO	in/out	The Snoop is returned.
SDONE	in/out	The Snoop is completed.
8. 64-Bit Expansion Signal		
Signal Name	**State Type**	**Description**
AD32~AD63	t/s	When the Protocol Analyzer PCI is in the 64Bits Transmission, they are the used Data Line and Address Transmission Line.
C/BE4~7	t/s	When the Protocol Analyzer PCI is in the 64Bits Transmission, they are the shared Input Signal and Output Signal for the Bit and the Protocol Analyzer.
REQ64	t/s	It is the Transmission Request in 64Bits.
ACK64	t/s	It is the Transmission ACK in 64Bits.
PAR64	t/s	It is the Parity Check.

Table1: Protocol Analyzer PCI Signal

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Use the ZEROPLUS Logic Analyzer to measure the Protocol Analyzer

PCI

Because the Protocol Analyzer PCI has many pins, it only can support the ZEROPLUS Logic Analyzer LAP-B Series at present. The below is an example to use the ZEROPLUS Technology LAP-B (702000) to do the measurement.

The test object is the transmission condition between the PCI Slot and PCI Data Card on the motherboard. For the hardware, the test object is connected to the Logic Analyzer through the PCI Measurement Fixture of ZEROPLUS Technology.

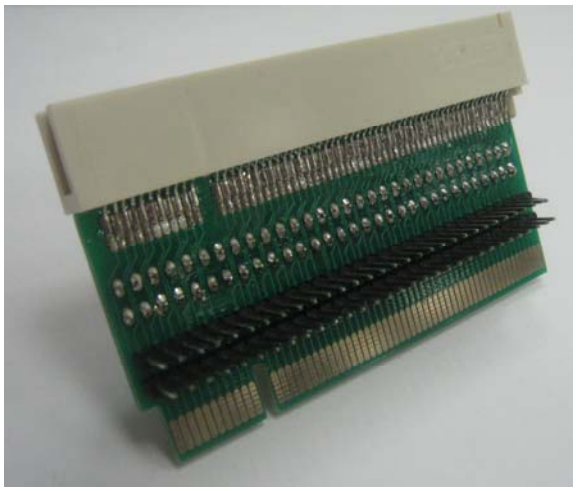

Figure 2: Protocol Analyzer PCI Measurement Fixture of ZEROPLUS Technology

Use the test cable of ZEROPLUS Logic Analyzer to connect the Logic Analyzer to the PCI Measurement Fixture:

Figure 3: Use the PCI Measurement Fixture and the Test Cable of ZEROPLUS Technology

After the signal connection is completed, connect the GND Line of the Logic Analyzer to the GND terminal of the motherboard; use the GND pin of the USB Port to connect to the other terminal.

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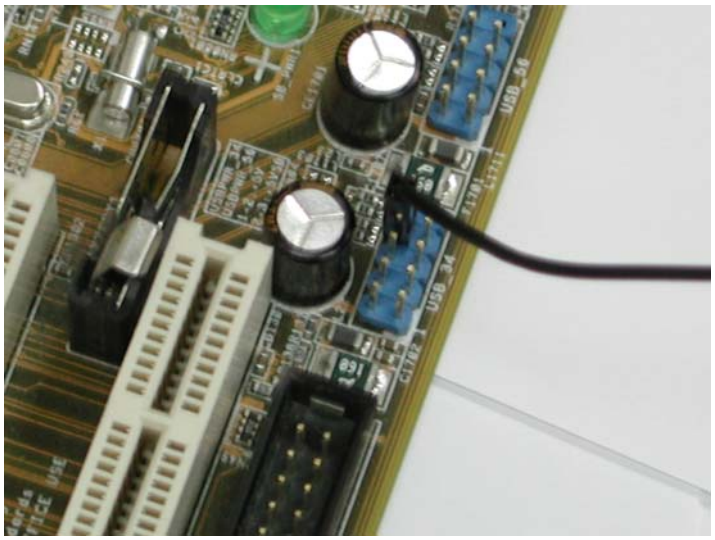

Figure 4: Connect the GND Line of the Logic Analyzer to the GND terminal of the motherboard.

When the test points of the Protocol Analyzer PCI have been connected to the LAP-B (702000) one by one, set the relative parameters in sequence.

- The RAM Size is 2M.
- The Sampling Frequency is 333MHz.
- The Trigger Condition is the CLK at the Rising Edge.

When the parameters have been set, the software can be activated to do analysis; the image is captured as below (Refer to *Figure 5*):

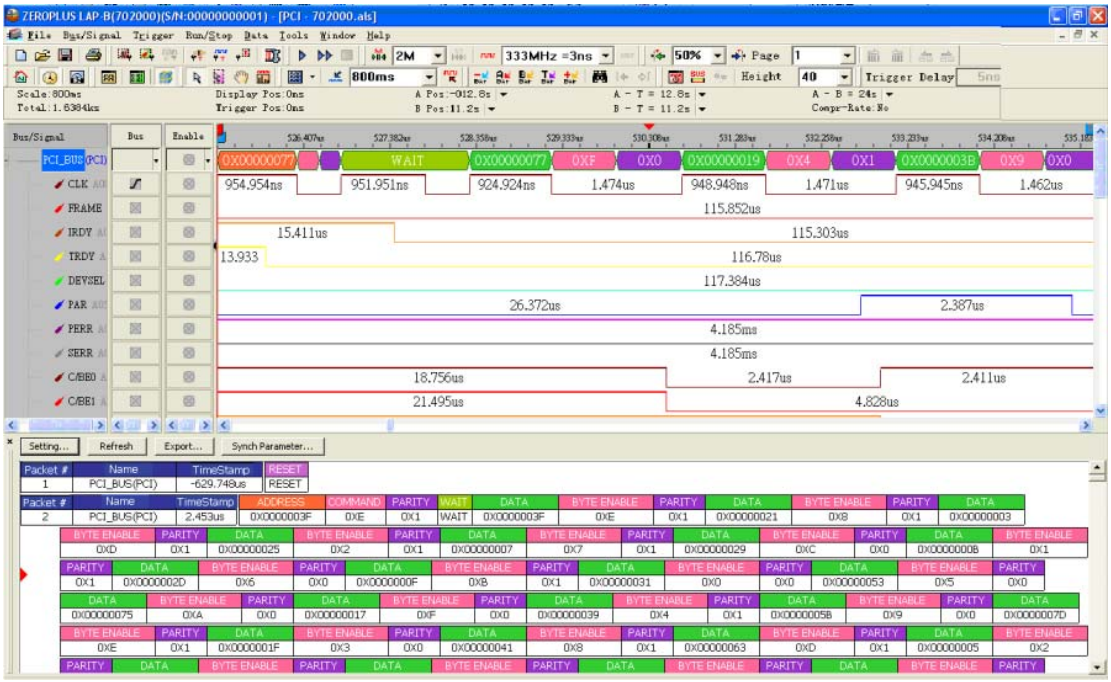

Figure 5: Use the ZEROPLUS Logic Analyzer to analyze the Protocol Analyzer PCI.

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The setting of Protocol Analyzer PCI Decoding Module of ZEROPLUS Logic Analyzer is simple and easy to understand; users only need to set the corresponding channels, and then press OK to start analyzing (*Figure 6*).

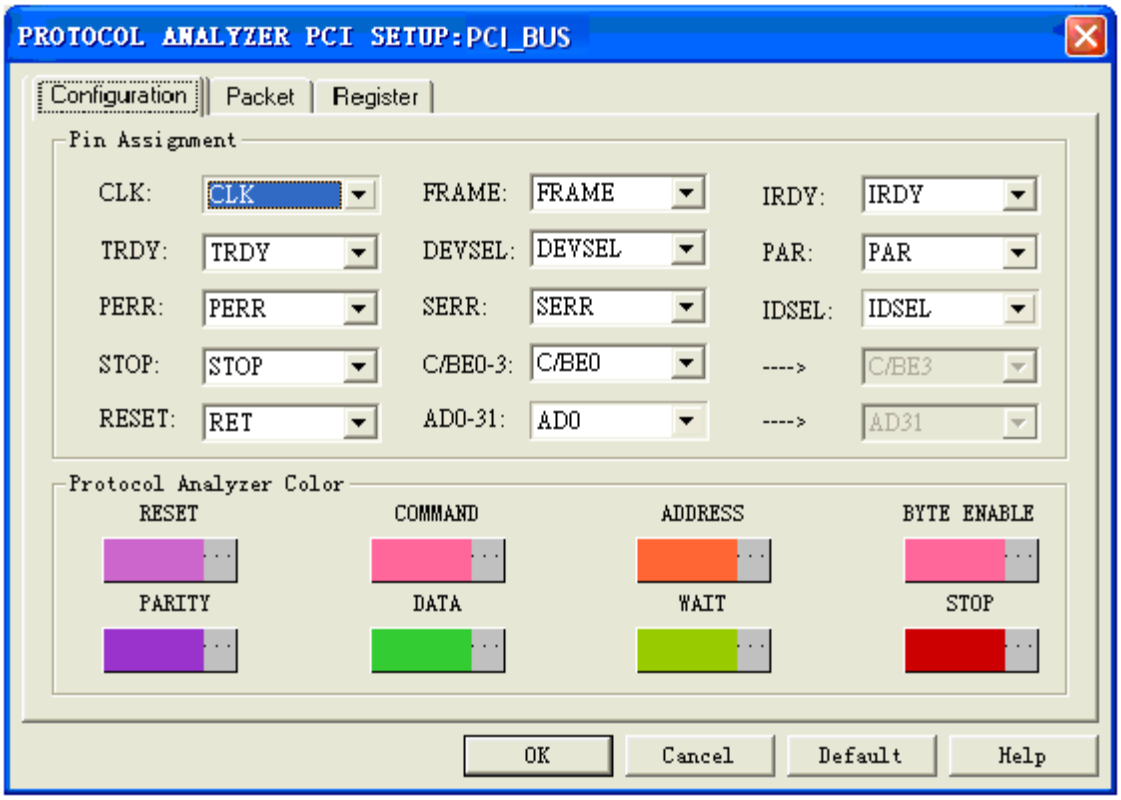

Figure 6: Protocol Analyzer PCI Setup Dialog Box

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The Packet Format Description of Protocol Analyzer PCI Decoding Module of ZEROPLUS Technology

Users can decode the RESET, COMMAND, ADDRESS, BYTE, PARITY, DATA, WAIT and STOP of the Protocol Analyzer PCI according to the Protocol Analyzer PCI Decoding Module of ZEROPLUS Technology. The below is the introduction for the above packets:

- **RESET:** It is the RESET Signal of the system. In any case, if the RESET is “0”, it denotes that the PCI device is doing the Reset action. When the RESET is changed into “1”, it denotes that the Reset action has ended.
- **COMMAND:** It can be divided into the following different COMMAND according to the sequence of C/BE3 ～ C/BE0.
- **Interrupt ACK:** It is a kind of Read Command, and the Master Device reads the interruption vector of the device which has applied for the interruption.
- **Special Period:** It is a kind of Broadcast Mechanism in the Protocol Analyzer PCI, and it can transmit different message from the Slave Device.
- **I/O READ/ I/O WRITE:** It is used to store the I/O Address Space.
- **RESERVE:** In order to add the extensibility for the PCI Command, reserve the Command Bit; at that moment, all the devices of the Protocol Analyzer PCI won’t cause the relative actions for this Command.
- **Memory Read/ Write:** It is used to read or write the I/O Device which is mapped from Address to Memory Space.
- **Configuration Read/Write:** It specially stores the Configuration Setting of the Device.
- **Multiple Memory Read:** This Command can make the Memory Controller search the Cache Line firstly when the quantity of Data Transmission is so larger that many pieces of Cache need to be used.
- **Dual Address Period:** It allows the 32Bits Protocol Analyzer to use the 64Bits Address to do the communication for the Device.
- **Single Memory Read:** The difference between this Command and the Memory Read is that it only reads one Cache Line before the completion, so it can increase the efficiency of the Memory Transmission.
- **Memory Write and Void:** The difference between this Command and the Memory Write is that it is written according to only one Cache Line; it will force the Cache Controller to clear the corresponding written area.

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C/BE[3:0]	PCI 命令 Command
0000	Interrupt ACK
0001	Special Period
0010	I/O Read
0011	I/O Write
0100	Reserve
0101	Reserve
0110	Memory Read
0111	Memory Write
1000	Reserve
1001	Reserve
1010	Configuration Read
1011	Configuration Write
1100	Multiple Memory Read
1101	Dual Address Period
1110	Single Memory Read
1111	Memory Read and Void

Table 2: PCI Commands List.

- **ADDRESS:** It consists of AD0～AD31, and it denotes the using ADDRESS when the Protocol Analyzer PCI transmits the data.
- **BYTE:** It is the BYTE ENABLE, and it denotes that the DATA BYTE of this data is valid or not.
- **PARITY:** It is the PARITY Check, and it is used to judge whether the content of the data is correct or not when transmitting the Data.
- **DATA:** It consists of AD0～AD31, and it denotes the transmitted DATA for the Protocol Analyzer PCI. When starting decoding, the AD0～AD31 will transmit the ADDRESS firstly; after confirming the ADDRESS Decoding finished, it starts to denote the content of DATA.
- **WAIT:** When the RESET is “1”, the FRAME and the IRDY are “1”; it denotes that the Protocol Analyzer is in the IDLE state, and the Module displays WAIT, as well as the COMMAND is judged as the READ state. It starts decoding from the first Rising Edge of the CLK following the Falling Edge of FRAME.
- **STOP:** The Protocol Analyzer PCI uses the Master and Slave Device to start the Data Transmission. STOP is sent to the Master Device when the Slave Device stops transmitting the data; it denotes that it is an application for stopping Data Transmission.

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Conclusion

Although the Protocol Analyzer PCI is complex, the powerful function is also used widely. When starting developing, using the suitable instrument can get twice the result with half the effort. The operation of the Protocol Analyzer PCI Decoding Module of ZEROPLUS Logic Analyzer is very convenient; it can display the complicated decoding process on the computer screen quickly according to the Software; engineers needn't spend much time on the analysis of the protocol. And ZEROPLUS Logic Analyzer can support fifty Protocol Analyzer Modules at present; it also can support the common Protocol Analyzer on the market. ZEROPLUS Technology also provides the Customization Module Service for customers, and it can help engineers do the development project with great facility. If you want to know more detailed information, please visit our website, www.ZEROPLUS.com.tw.

Reference：

PCI-E + SATA+ USB 2.0+IEEE 1394+ Bluetooth PC Hardware Interfaces – A Developer's Reference Author：Michael Gook