



LPT Measurement and Analysis

Brief Introduction of LPT

A kind of parallel interface has been added in the Personal Computer since the eighties. With the help of the interface, users can connect a printer to the PC. Because the interface is designed for printing, it is named as LPT (Line Printer Terminal Port).

The traditional LPT (SPP, Standard Parallel Port) is mainly used for transmitting data. However, it also can be used for inputting a small part of data. The modified LPT includes Bi-directional Port, Enhanced Parallel Port and Extended Capabilities Port. At first, those modified ports were the single solutions, which were proposed by the manufacturers. And later, they were integrated into the IEEE 1284 standards by IEEE (Institute of Electrical and Electronics Engineers).

With regard to the structure of the hardware, the LPT has 8-bit data bus, 5-bit signal bus for monitoring statuses and 4-bit control signal bus, and it adopts the DB-25 connector.

LPT adopts the TTL Voltage Level. However, the length of the LPT cable is limited because of the worse anti-noise capability of the TTL interface.

With regard to the software, the LPT uses the Input/Output Address Space of a Register. The Register of the Port is addressed according to its base position. And the common Base Address includes 3BCh, 378h and 278h. The LPT can be interrupted by the hardware; it is usually the IRQ5 or IRQ7. And in the enhanced operating mode, the function of DMA (Direct Memory Access) can be used further.



LPT Pin

The traditional LPT is the SPP (Standard Parallel Port). The corresponding relationship of the Pin No., Signal Function/ Name and Register are shown as *Figure 1* and *Table 1*.

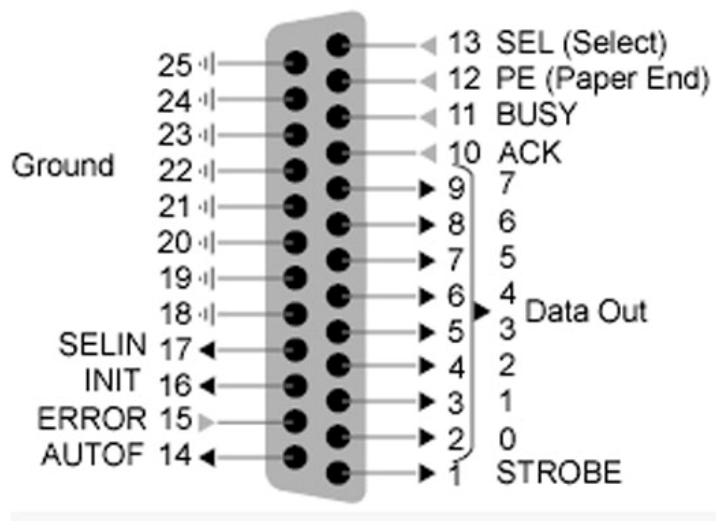


Figure 1: LPT Pin Diagram

DB-25 Pin No.	Function/ Name of the Signal	Register
1	Strobe#	CR.0\
2	Data0	DR.0
3	Data1	DR.1
4	Data2	DR.2
5	Data3	DR.3
6	Data4	DR.4
7	Data5	DR.5
8	Data6	DR.6
9	Data7	DR.7
10	Ack#	SR.6
11	Busy	SR.7
12	PE(Paper End)	SR.5
13	Select	SR.4
14	AUTOFF(Auto Feed)	CR.1\
15	Error#	SR.3
16	Init#	CR.2
17	Select In#	CR3.\
18~25	GND	N/A

Table 1: Comparison Table for LPT Pin, Signal Function/ Name and Register



The Standard Parallel Port has three 8-bit Registers, and the three Registers occupy three continuous and adjacent addresses, which start from the Base Addresses (3BCh, 378h, 278h) of the Port.

DR (Data Register) is the Output Port.

The address of DR is equal to BASE plus zero. The written data in the Register will be outputted to Data [7:0], which shows the status of the outputted data.

SR (Status Register) is the Input Port.

The address of SR is equal to BASE plus one. The Register represents the Status Signal of the Printer; the function for each bit of the SR is described as below.

SR.7(SR bit7): Busy; it is denoted by the reverse level. That is to say, when the level of the cable is Low Level, the bit of the Register will be set to Positive Logic, which denotes that the next byte can be outputted.

SR.6: Ack (Acknowledge); it denotes the status level on the Ack# Pin. When the status level is Logic 0, it represents Acknowledge.

SR.5: PE (Paper End); it denotes the status level on the PE Pin. Specifically, it shows the numbers of the paper in current printer. When the status level is Logic 1, it denotes the printer is lack of paper.

SR.4: Select; it denotes the connection status of the printer. When the status level is Logic1, it denotes the printer has been connected presently.

SR.3: Error; it denotes the status level on Error# Pin. Specifically, it denotes the abnormal operating status of the printer. When the status level is Logic 0, it denotes that the error appears in the current printer.

SR.2: PIRQ; it denotes the Interrupt Flag of Ack#. That is to say, when Ack# produces a Hardware Interrupt, the bit will be set to Logic 0; when the hardware is set again and the Status Register is read, the bit will be set to Logic 1.

SR [1:0]: Reserve

CR (Control Register) is the Output Port

The address of CR is equal to BASE plus two. The Register denotes the control status of the Printer; the function for each bit of the CR is described as below.

CR [7:6]: Reserve

CR.5: Direction; it denotes the control bit of the transmission direction. It is only limited in the Port of PS/2 or Bi – Di.

CR.4: AckINTEN (Acknowledge Interrupt Enable); when the bit is Logic 1, it denotes that the interrupt is allowed after the Ack# signal appears.

CR.3: Select In.; when the bit is Logic 1, it denotes that the Printer is allowed to work in the Centronics mode.

CR.2: Init; when the bit is Logic 0, it denotes that hardware of the Printer has been reset.

CR.1: Automatic line feed (AUTOF) ; when the carriage – return bit is received, the Line-feed signal will be produced automatically; the signal and the bit are also named AutoLF or AutoFDXT.

CR.0: Strobe; the bit is used as the Strobe signal of the output data.

Introduction of IEEE1284 Standard

IEEE1284 Parallel Interface Standard describes SPP, EPP and ECP. And the Standard defines five kinds of Data Transmission Mode, which are described as below:



Compatibility Mode: It is the default mode of LPT. When the mode is initialized or before the mode is changed, the default mode is still Compatibility Mode.

Nibble Mode: The SR [7:4] in DB-25, namely, 11, 12, 13 and 15 Pin, can be used to transmit four bit at a time. Although the mode can be used in all Ports, the transmission rate is very low (the highest transmission rate is 50KBps). The mode is complementary to the Compatibility Mode, but they cannot be used at the same time, and the switch action between them needs to be controlled by the Host.

Byte Mode: The Data0 ~ Data7 in DB-25 are defined as Bi-directional Port directly, and the Bi-directional Handshake Transmission can be realized by matching them with other control cables (Strobe#, AutoF#, Select In#, Init#, Ack#, Busy, PE, Select and Error); the highest transmission rate is 150KBps.

EPP Mode: When the IEEE 1284 was not adopted formally, Intel, Xircom and Zenith Data System have developed the EPP (Enhanced Parallel Port) protocol, which is mainly used to increase the efficiency of data transmission.

The EPP mode has three features as below:

1. EPP mode supports Addressing function, which can make the peripheral devices on the bus own themselves ID Codes.
2. CPU does not take charge of the low level work of Handshake Control, but shift the work onto the hardware.
3. The 8-bit bi-directional transmission rate can be up to 2Mbytes/s.

ECP Mode: ECP mode is proposed by Hewlett-Packard (HP) and Microsoft. It is used for the communication among the peripheral devices of the Printer and the Scanner. The ECP mode not only has the features of EPP mode, but also has the below-described features:

1. The Receiving Devices must have the FIFO Memory above 16Byte, and the Memory is used as the Data Buffer for the purpose of improving the transmission rate.
2. ECP mode supports the Data Compression Technology of RLE (Run Length Encoding).
3. ECP mode supports the DMA (Direct Memory Access).

No matter which Transmission Mode is used, when the machine is started, it must run firstly in the Compatibility Mode. And then it will enquire whether the peripheral devices comply with IEEE 1284 specification through some programs; if the peripheral devices do not comply with IEEE 1284 specification, it will keep the traditional Parallel Port; if the peripheral devices do comply with IEEE 1284 specification, the peripheral devices will respond a string of character string of ASCII in order to inform the types of the peripheral devices, command and the working mode, and then the transmission mode of the Parallel Port can be decided.



Besides the above-described main IEEE 1284 standards, there are other several standards to do the further instructions.

1. IEEE P1284.1 Standard for Information Technology for TIP/SI: According to a kind of Bi-directional Interface based on NPAP (Network Printing Alliance Protocol), the IEEE P1284.1 is a kind of System/ Printer Interface, which is not relative to transmission.
2. IEEE P1284.2 Standard for Test, Measurement and Conformance to IEEE Std. 1284: It is used to check whether the devices, the ports and the cables comply with the IEEE 1284 standard.
3. IEEE P1284.3 Standard for Interface and Protocol Extensions to IEEE Std. 1284 Compliant Peripheral and Host Adapter Ports: The standard is developed for sharing the parallel port in a daisy chained or switched (multiplexed) architecture; it is a necessary application and driver software interfaces required to implement drivers for IEEE 1284 compliant peripherals.
4. IEEE P1284.4 Standard for Data Delivery and Logical Channels for IEEE Std. 1284 Interfaces: With regard to the Packet Protocol and the Logic Channel Structure of 1284 device, the IEEE P1284.4 corresponds to the Transmission and Conversation Layer in OSI model and it provides the Configuration, Data Flow Control and Data Transmission as well as the Service Detection of User Terminals.



LPT Actual Measurement

ZeroPlus Technology Logic Analyzer can support the function of decoding LPT signal, and then measure the transmission status between PC and Label Machine through the fixture.

Figure 2 shows the LPT Test Tool. With the help of the tool, DB-25 channels can be connected to Logic Analyzer respectively.

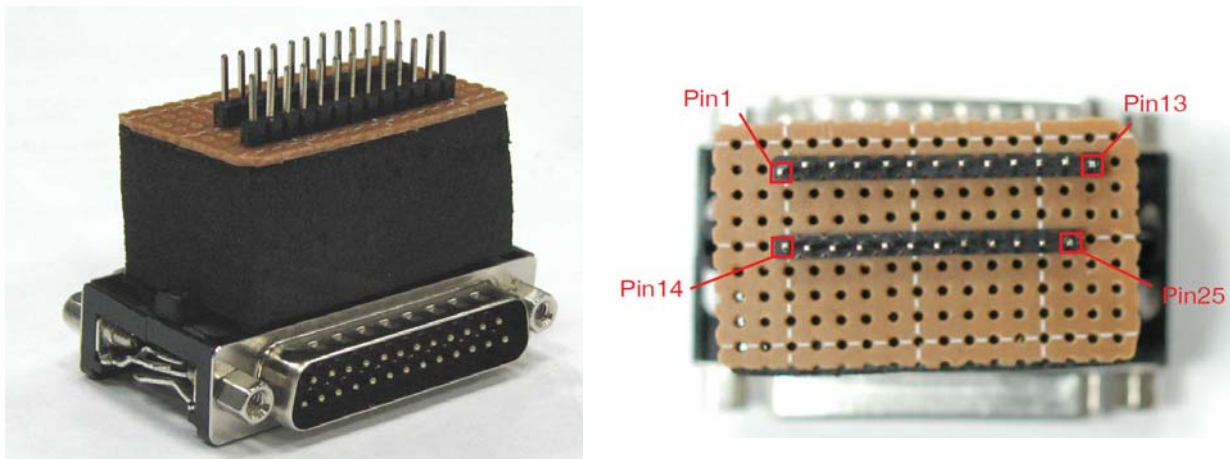


Figure 2: LPT Test Tool

When the LPT ports on PC are connected to one side of the tool through DB-25 cables, the other side should be connected to the Label Machine through DB-25 cables.

When using the ZeroPlus Logic Analyzer, the channels in LPT (DB0 ~ DB7, STOBE, ACK, BUSY, PE, SELECT, AUTO FEED, ERROR and SELECT IN) should be connected to the Logic Analyzer. The A0 ~ A7 on the Logic Analyzer are connected to Pin 2 ~ Pin9 (please refer to the *Table1* to learn the Pin and the name) on the tool respectively; B0 is connected to Pin1; B1 is connected to Pin10; B2 is connected to Pin11; B3 is connected to Pin12; B4 is connected to Pin13; B5 is connected to Pin14; B6 is connected to Pin15; B7 is connected to Pin17; GND ports of Logic Analyzer are connected to Pin24 and Pin25.

The completed connection is shown as *Figure 3*.

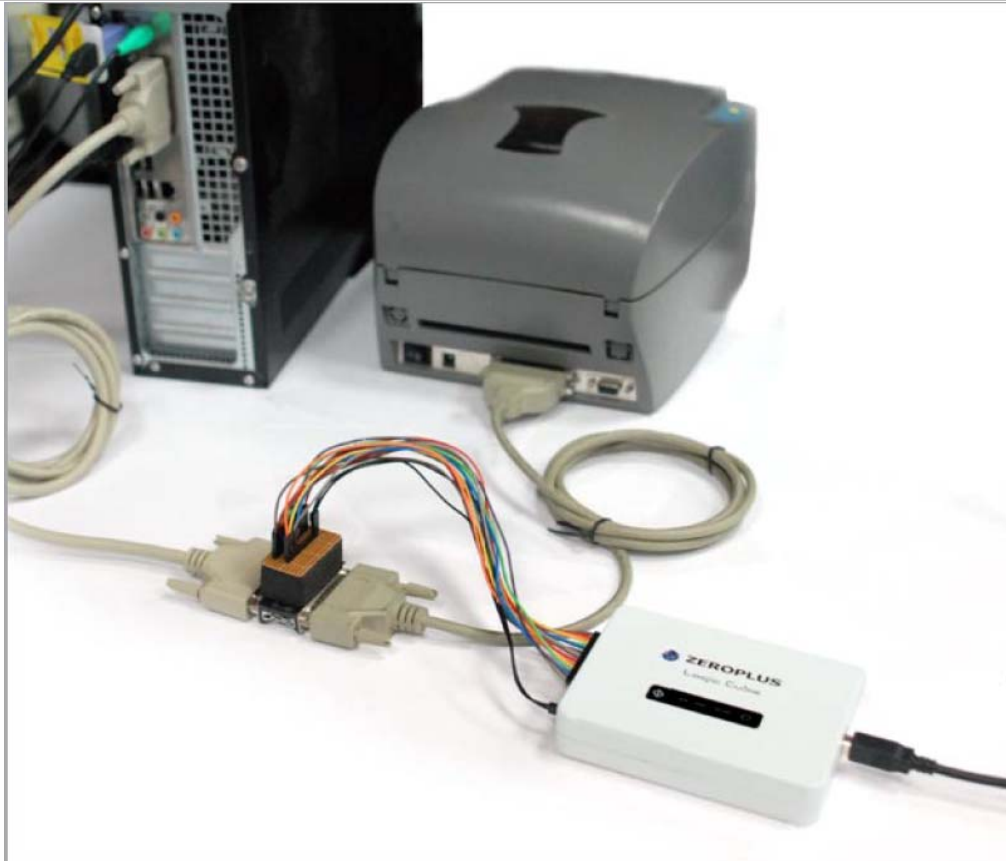


Figure 3: Completed Test Environment

When the connection is completed, the software of ZeroPlus Logic Analyzer can be activated to test the signal (If users want to learn the operating instructions of the Logic Analyzer, please visit the website of ZeroPlus Technology, www.zeroplus.com.tw). The captured waveform is shown as *Figure 4*.

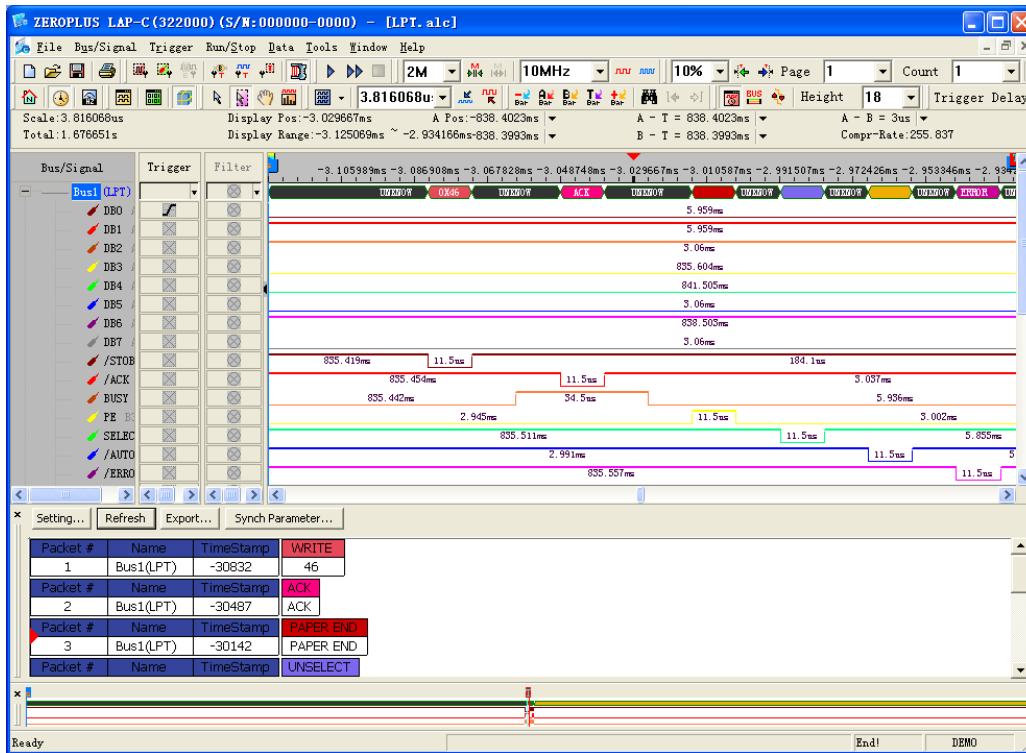


Figure 4: Captured Waveform of LPT Signal

The Protocol Analyzer LPT of ZeroPlus Technology Logic Analyzer not only can analyze the packet of the signal automatically, but also can set the LPT Mode (SPP, EPP and ECP) according to the connected LPT Port.

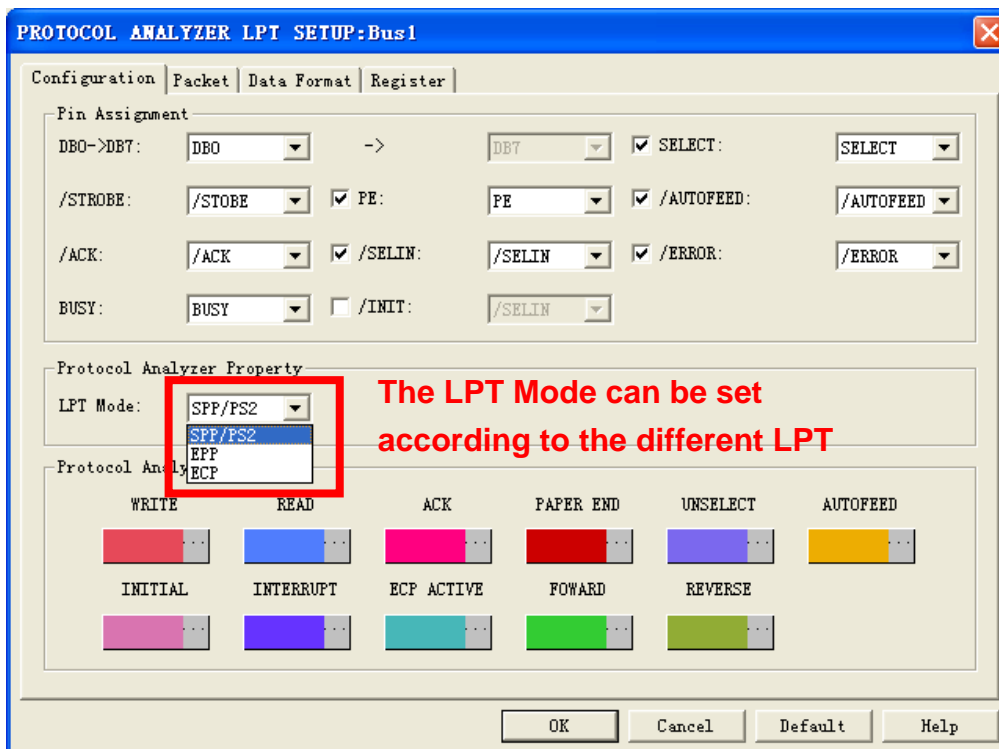


Figure 5: LPT Configuration Dialog Box (in SPP/PS2 Mode)



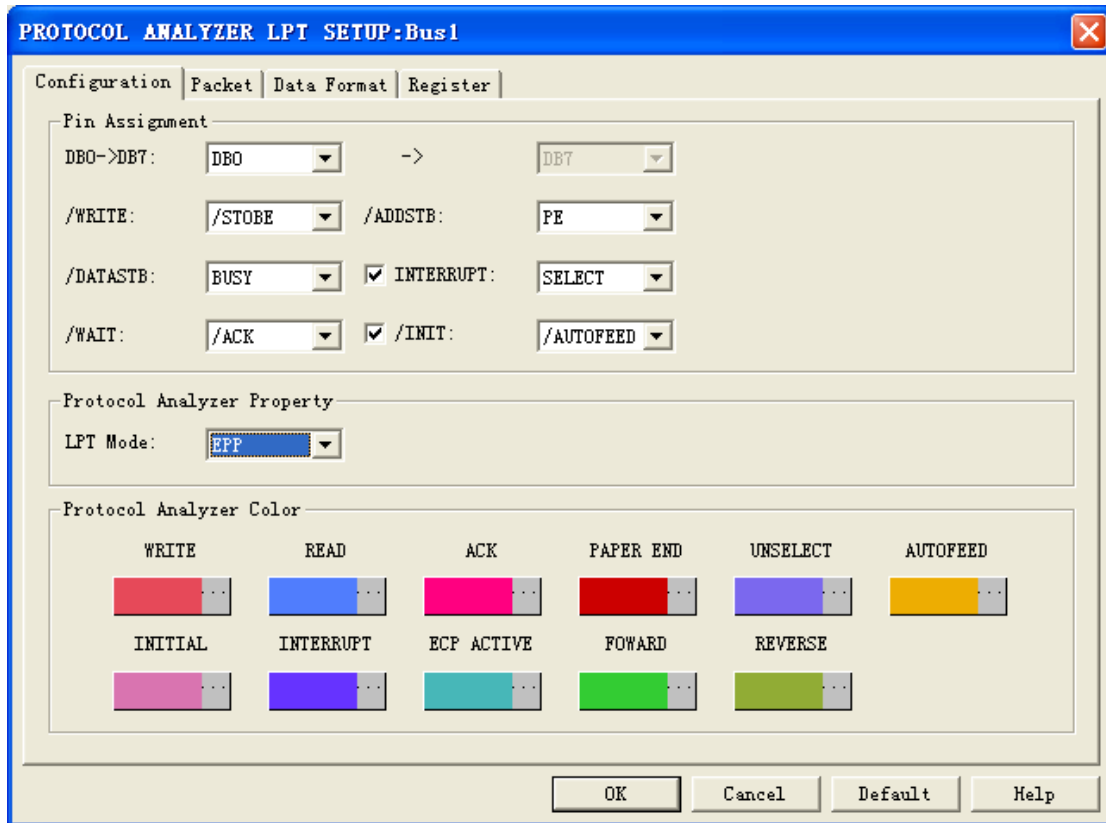
In the EPP and ECP Mode, as the Pin No. and the corresponding signal name are changed, it is necessary to notice the Pin Name and the corresponding Signal Name when doing the test. The tested Pins in EPP and ECP Modes will be described as the below tables.

EPP Mode

DB-25 Pin No.	SPP Signal Name	EPP Signal Name	Description
1	Strobe	Write	Low Level denotes a Write Period; High Level denotes a Read Period.
14	Auto	DataStb	Data Strobe: It is set to Low Level in the Data Transmission Period.
17	SelectIn	AddStb	Address Strobe: It is set to Low Level in the Address Transmission Period.
16	Init	Reset	Reset: When it is in Low Level, the peripheral devices will be switch to the Compatibility Mode.
10	Ack	INTR	Peripheral Interrupt: It is used to produce an interrupt signal and transmit the signal to the Host.
11	Busy	Wait	Handshake Signal: When it is in Low Level, it denotes a period can be activated; when it is in High Level, it denotes a period will be ended.
2~9	Data[0:7]	AD[0:7]	Bi-directional Address / Data Bus
12	Paper End	Ack Data Req	It is decided by the developer of the peripheral devices.
13	Select	Xflag	It is decided by the developer of the peripheral devices.
15	Error	Data Avail	It is decided by the developer of the peripheral devices.



LPT Configuration Dialog Box in EPP Mode



ECP Mode

DB-25 Pin No.	SPP Signal Name	ECP Signal Name	Description
1	Strobe	Host Clk	Data Strobe Signal: It is used to coordinate with the Periph Ack Signal to transmit the forward output.
14	Auto LF	Host Ack	It denotes the type of the period in Forward Transmission Mode. When transmitting the reverse data, it coordinates with Periph Clk Signal and functions as an Ack Signal.
17	Select In	1284 Active	ECP mode indicator: When the signal is in Low Level, ECP mode will be switched to the Compatibility Mode.
16	Init	Reverse Request	Reverse Request: When it is in Low Level, it denotes the channel has been switched to Reverse Mode.
10	Ack	Periph Clk	Data Strobe Signal: It is used to coordinate with the Host Clk Signal to transmit the reverse output.
11	Busy	Periph Ack	It denotes the status of the Command/ Data in Reverse Transmission Mode. When transmitting the forward data, it coordinates with Host Ack Signal and functions as an Ack Signal.
12	Paper End	Ack Reverse	Ack Reverse: It is switched to the Low Level for the purpose of responding the Reverse Request signal.
13	Select	Xflag	ECP Mode Ack
15	Error	Periph Request	It denotes a Notice Request for the Host.
2~9	Data[0:7]	Data[0:7]	Bi-directional Data Channel



LPT Configuration Dialog Box in ECP Mode

PROTOCOL ANALYZER LPT SETUP: Bus 1

Configuration | Packet | Data Format | Register

Pin Assignment

DB0->DB7: DBO -> DB7 X-FLAG: /AUTOFEED

PERIPHCLK: /ACK HOSTCLK: /STOBE 1284 ACTIVE: /SELIN

HOSTACK: SELECT ACKREVERSE: PE PERIPHREQUEST: /ERROR

/PERIPACK: BUSY REVERSEREQUEST: /SELIN

Protocol Analyzer Property

LPT Mode: ECP

Protocol Analyzer Color

WRITE	READ	ACK	PAPER END	UNSELECT	AUTOFEED
INITIAL	INTERRUPT	ECP ACTIVE	FORWARD	REVERSE	

OK Cancel Default Help



Conclusion

The LPT was early used in many fields, where the large number of transmission was required, for example, Printer or Plotter. Besides the Printer, the LPT was used for some other devices gradually, such as Electronics Lock, Scanner, and Storage Media of ZIP DRIVE. With the unceasing evolution of the interface, LPT is being replaced by USB gradually. However, in the application for the automatic control, LPT Port is still one of the indispensable communication interfaces.

Zeroplus Technology Logic Analyzer has issued more than fifty Protocol Analyzers. When engineers analyze the Protocol Analyzer signals, the time of development can be reduced through the automatic decoding function of the software and the product can come into the market earlier. At the same time, with the help of the software, it is unnecessary to decode the signal with manual mode when facing various digital signals. If you want to learn more introductions about the Zeroplus Logic Analyzer, please visit the website of Zeroplus Technology, www.zeroplus.com.tw.