中和市建八路 123 號 2F
電話：886-2-66202225
傳真：886-2-22234362
www.zeroplus.com.tw
2F., No.123,Jian Ba Rd,
Chung Ho City, Taipei Hsien, R.O.C.
Tel: 886-2-66202225
Fax: 886-2-22234362

JTAG Measurement and Analysis

Brief Introduction of JTAG

JTAG (Joint Test Action Group) is a kind of interface, which is specially used for programming and testing the circuit board. JTAG Interface Technology, which is specified by IEEE-1149.1 Boundary Scan Architecture Standard, belongs to a kind of synchronous serial interface. Further, the feature of the JTAG interface is that a controller can connect to multiple devices to perform the test.

JTAG Interface mainly consists of the following signals:

TCK (Test Clock): It is the data synchronization signal, which is produced by the controller, and its frequency can be up to 16MHz.

TMS (Test Mode Select): It is used for selecting the test device, and it is produced by the controller.

TDI (Test Data Input): It is used to receive the data which is transmitted by the device from the controller.

TDO (Test Data Output): It is used to transmit the data of the device from the controller.

TRST (Test Logic Reset): It is used to reset the interface device, and it is produced by the controller.

It is noticed that the above-described signals are one-way transmission signals. A TAP (Test Access Prot) is formed by those signals, and the DUT (Device Under Test) is connected to the controller with the TAP. Further, the controller produces the test signals mainly depending on the test program which is defined by the manufacturer of the DUT, and then the tested result is compared with the sample. As long as the DUT accords with the JTAG specifications, a controller can connect to multiple devices in serial through the TAP.

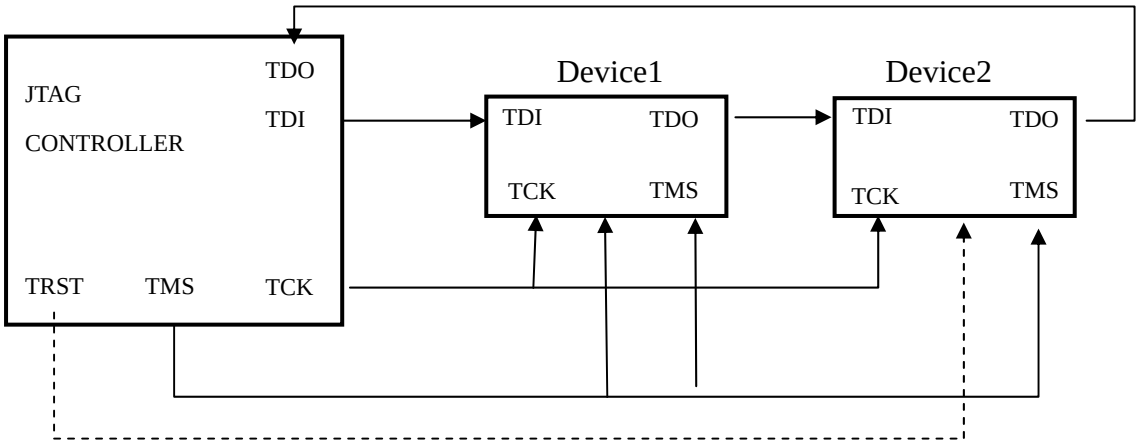


Figure 1: JTAG Interface Device in Serial

中和市建八路 123 號 2F
電話：886-2-66202225
傳真：886-2-22234362
www.zeroplus.com.tw
2F., No.123,Jian Ba Rd,
Chung Ho City, Taipei Hsien, R.O.C.
Tel: 886-2-66202225
Fax: 886-2-22234362

A Digital Circuit has input, output and two-way communication. There is a B/S Test Cell (B/S Cell) added between the external output of the device and the logic device. And the TAP controller can scan those cells. That is the so-called Boundary Scan as the following *Figure 2*. When the test mode is started, the TAP controller can make the signal and the external output lose the connection in logic, thereby set up the action of the input and then read the result. In fact, such action mode is the thing that should be done by the test device.

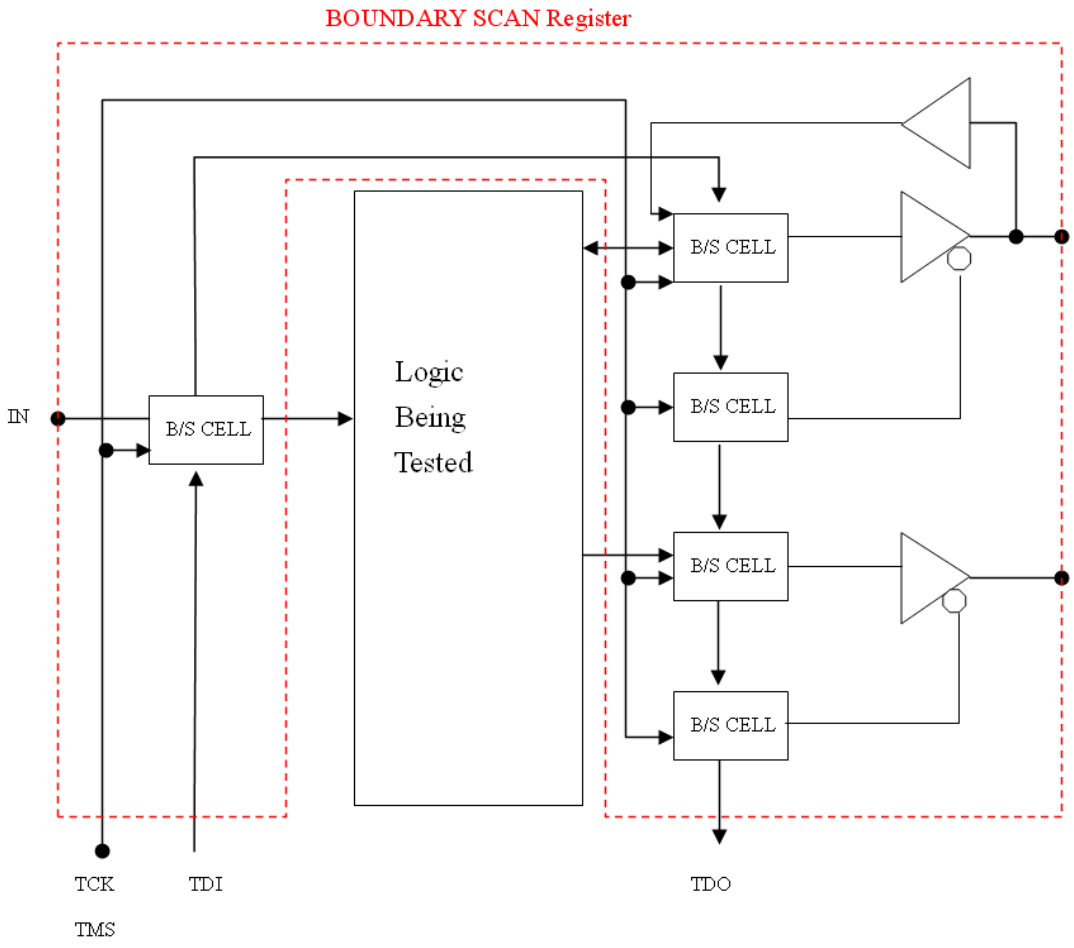


Figure 2: Connecting to the Scan Cell

中和市建八路 123 號 2F
電話：886-2-66202225
傳真：886-2-22234362
www.zeroplus.com.tw
2F., No.123,Jian Ba Rd,
Chung Ho City, Taipei Hsien, R.O.C.
Tel: 886-2-66202225
Fax: 886-2-22234362

The device that supports the JTAG needs to comprise the following test elements.

TAP (Test Access Port)	TAP consists of four signals.
TAP Register Controller	
IR (Instruction Register)	It is used to receive the serial number which is inputted by the TDI, and the instruction code is used to select the test action to be performed, or select the Test Data Register to be used.
Test Data Register	A device must have three registers, namely, **BPR** (Bypass Register), **DIR** (Device Identification Register) and **BSR** (Boundary Scan Register).

The IR (Instruction Register) and the Test Data Register belong to the different Shift Register; both of them are connected with each other in a parallel mode. Further, the TDI signal is connected to the Input Port and the TDO signal is connected to the Output Port. When one pulse signal appears in the TCK Port, the data in the Shift Register will move one bit.

The length of the BPR (Bypass Register) is only one bit. When other registers don't perform the exchange, the BPR will function as the fastest bypass to transmit the serial data.

BSR (Boundary Scan Register) is a longer Shift Register, wherein every bit is the boundary cell corresponding to the input and output signal of the processor. As to the two-way signal or the consisted group, besides the Register Information Cells which correspond to the external signal, there are Control Cells which are used to set the operation mode for the Information Cells.

The length of the DIR (Device Identification Register) is 32bits. The content of the DIR includes the identification bit of the manufacturer, device code and the version number. However, the TAP controller can not identify the type of the DUT until there is the DIR Register.

The IR is used to store the implemented test instructions, and the length of the IR depends on the DUT. Further, all devices must support the following instructions, namely, BYPASS, IDCODE, SAMPLE/PRELOAD and EXTEST.

中和市建八路 123 號 2F
電話：886-2-66202225
傳真：886-2-22234362
www.zeroplus.com.tw
2F., No.123,Jian Ba Rd,
Chung Ho City, Taipei Hsien, R.O.C.
Tel: 886-2-66202225
Fax: 886-2-22234362

Instruction Explanation of BYPASS, IDCODE, SAMPLE/PRELOAD and EXTEST:

BYPASS	The content of the BYPASS code consists of 1, and it is mainly used to connect the1-bit BPR to supply the fastest path for the Bypass Device.
IDCODE	It is the identification instruction. The two lowest bits of the instruction code are 10, and it is mainly used to connect the DIR to the interface and read the content of the register.
SAMPLE/PRELOAD	The two lowest bits of the instruction code are 01, and the function of the instruction is divided into two kinds. One is that when the TAP controller is in the Capture–DR status, the instruction can capture all external signals without affecting the operation of the device. The other is that when the TAP controller is in the Update–DR status, the instruction can shift data to the output of the processor by utilizing the EXTEST instruction.
EXTEST	The two lowest bits of the instruction code are 00. EXTEST instruction is used to test the external circuit, and in the process of the operation, the first written signal in the BSR will be shifted to the Output.

Besides the above-described four instructions, the IEEE1149.1 also provides the INTEST instruction for testing the internal logic of the device, but all devices don’t support the INTEST instruction.

When the TAP is powered on, it will return to the initial Test Logic Reset automatically. No matter what status the controller is in, as long as the high level of the TMS keeps more than 5 TCK periods, the controller will be forced to enter into the Reset status, however, sometimes it returns to the initial status through the TRST signal.

中和市建八路 123 號 2F
電話：886-2-66202225
傳真：886-2-22234362
www.zeroplus.com.tw
2F., No.123,Jian Ba Rd,
Chung Ho City, Taipei Hsien, R.O.C.
Tel: 886-2-66202225
Fax: 886-2-22234362

Introduction of the TAP Controller' s Statuses:

Run-Test-Idle Status	It is the middle status between the test operation and the implementation. In this status, the value of the registers can not be changed.
Shift-DR Status	In this status, the data from the TDI will be shifted to the TDO via the connected Shift Register.
Pause-DR Status	In this status, the controller will forbid any data to shift via the Shift Register.
Update-DR Status	When the negative conversion of the TCK appears, the signal from the Shift Register will be latched on the output of the test cell.
Capture-DR Status	The controller will load the SAMPLE instruction into the Shift Register.
Shift-IR Status:	A Shift Register is inserted between the TDI and the TDO in a serial way, but the former instruction still continuously works.

Those main controllers decide the operation of the test device. However, besides those statuses, there are many other statuses, such as Select-DR-Scan, Exit1-DR, Exti2-DR, Select-IR-Scan, Exit1-IR and Exti2-IR. *Figure 3* is the flow chart of the TAP controller status conversion.

中和市建八路 123 號 2F
電話：886-2-66202225
傳真：886-2-22234362
www.zeroplus.com.tw
2F., No.123,Jian Ba Rd,
Chung Ho City, Taipei Hsien, R.O.C.
Tel: 886-2-66202225
Fax: 886-2-22234362

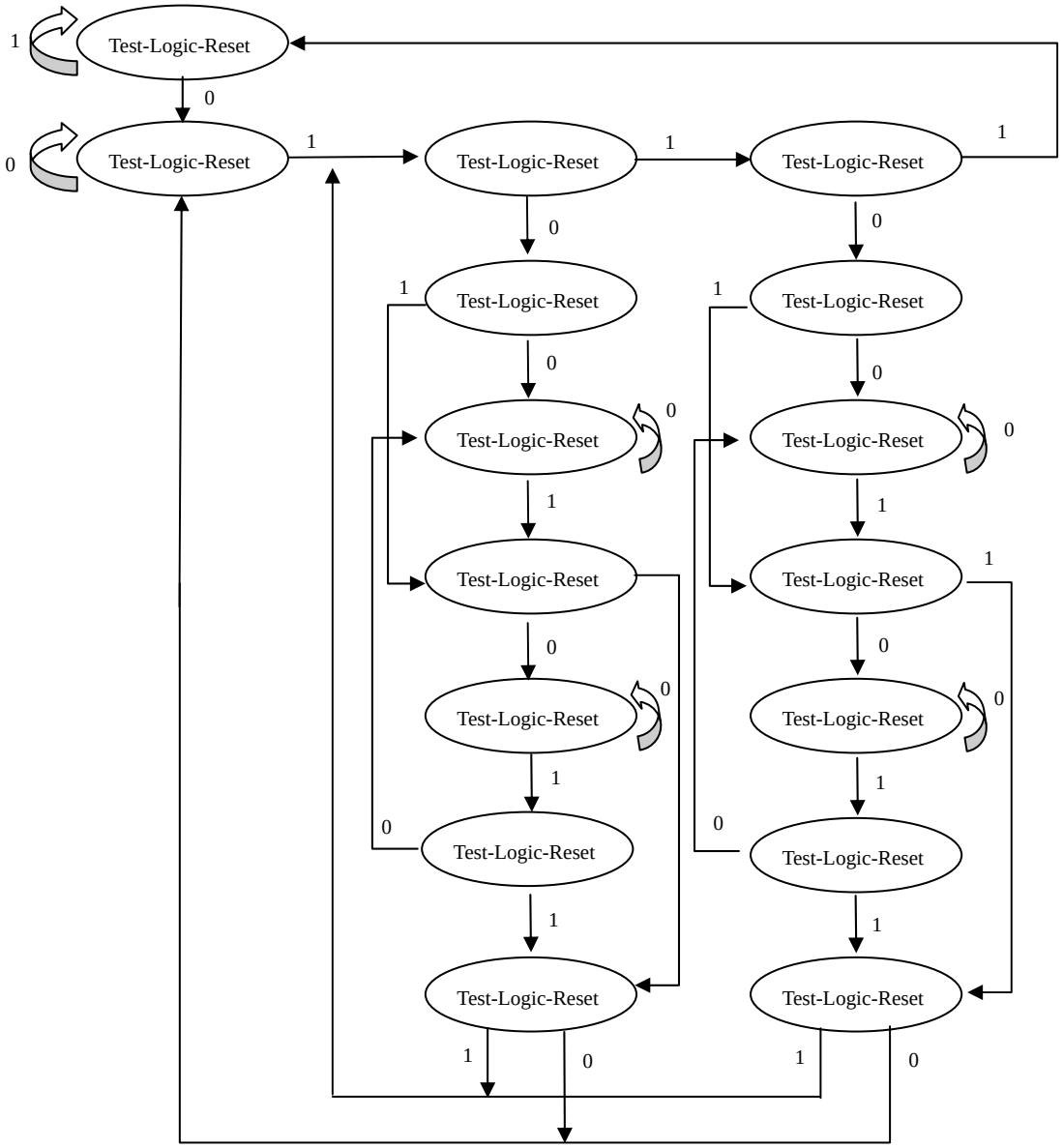


Figure 3: Flow Chart of the TAP Controller Status Conversion

At present, in accordance with the JTAG interface, there is a kind of special BSDL (Boundary Scan Description Language) developed to describe the device. Therein, the sequence and the characteristics between the information of every device in the Data Shift Register and the control cell have the unique feature, which needs to be supplied by the research and development manufacturer. At the same time, the JTAG interface not only is used to test devices, but also compile the different devices.

中和市建八路 123 號 2F
電話：886-2-66202225
傳真：886-2-22234362
www.zeroplus.com.tw
2F., No.123,Jian Ba Rd,
Chung Ho City, Taipei Hsien, R.O.C.
Tel: 886-2-66202225
Fax: 886-2-22234362

Actual Measurement of the JTAG Signal

Zeroplus Technology Logic Analyzer can support the decoding of the JTAG signals. When TCK, TMS, TDI, TDO and TRST on the TAP controller are connected to the Logic Analyzer, the Logic Analyzer can decode the signals.

Then the MAX II of Altera will be worked as the test aim of the JTAG to analyze the signal; the JTAG transmission is made for the MAX II by the GFEC USB-Download Cable and the signal is captured by the Zeroplus Logic Analyzer. *Figure 4* is the GFEC USB-Download Cable; *Figure 5* is the Altera MAX II development board, which is convenient for connecting with a Logic Analyzer. At the same time, there is a test fixture (refer to *Figure 6*) prepared for dividing the JTAG PORT（F）on the MAX II into two groups. One is connected to the JTAG PORT（M）of the USB-Download Cable, and the other is connected to the test cable of the Zeroplus Logic Analyzer.

Figure 4: GFEC USB-Download Cable

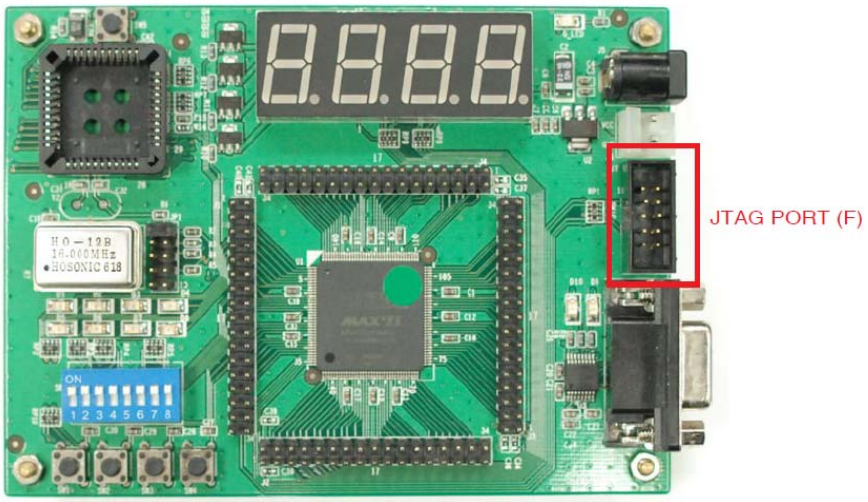


Figure 5: Altera MAX II Development Board

中和市建八路 123 號 2F
電話：886-2-66202225
傳真：886-2-22234362
www.zeroplus.com.tw
2F., No.123,Jian Ba Rd,
Chung Ho City, Taipei Hsien, R.O.C.
Tel: 886-2-66202225
Fax: 886-2-22234362

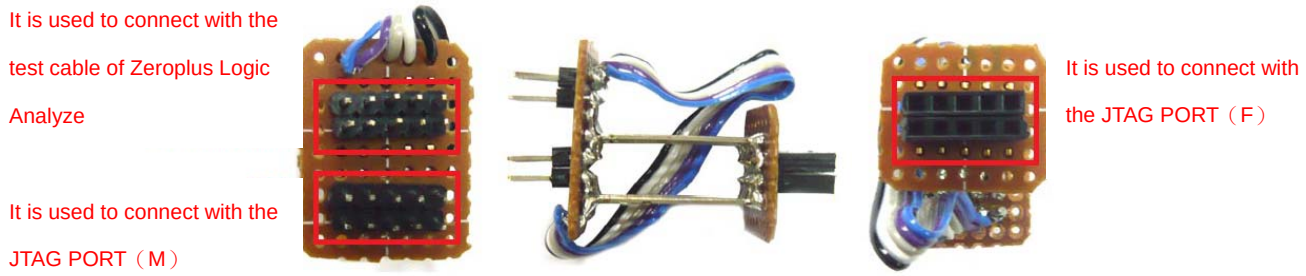


Figure 6: Signal Test Fixture

The JTAG PORT of the MAX II can be tapped through the Signal Tap Fixture (divide the signal into two parts). One is connected to the USB-Download Cable, and the other is connected to the Zeroplus Logic Analyzer through the test cable (the defaulted connection channel is A0~A3). *Figure 7* is a diagram of the completed connection.

Figure 7: Connected Test Circumstance

中和市建八路 123 號 2F
電話：886-2-66202225
傳真：886-2-22234362
www.zeroplus.com.tw
2F., No.123,Jian Ba Rd,
Chung Ho City, Taipei Hsien, R.O.C.
Tel: 886-2-66202225
Fax: 886-2-22234362

When the connection is finished, the software of the Zeroplus Logic Analyzer can be turned on to test the signal (the operation mode of the Zeroplus Logic Analyzer can refer to the Zeroplus Technology Website, www.zeroplus.com.tw), and the captured waveform is shown as the *Figure 8*.

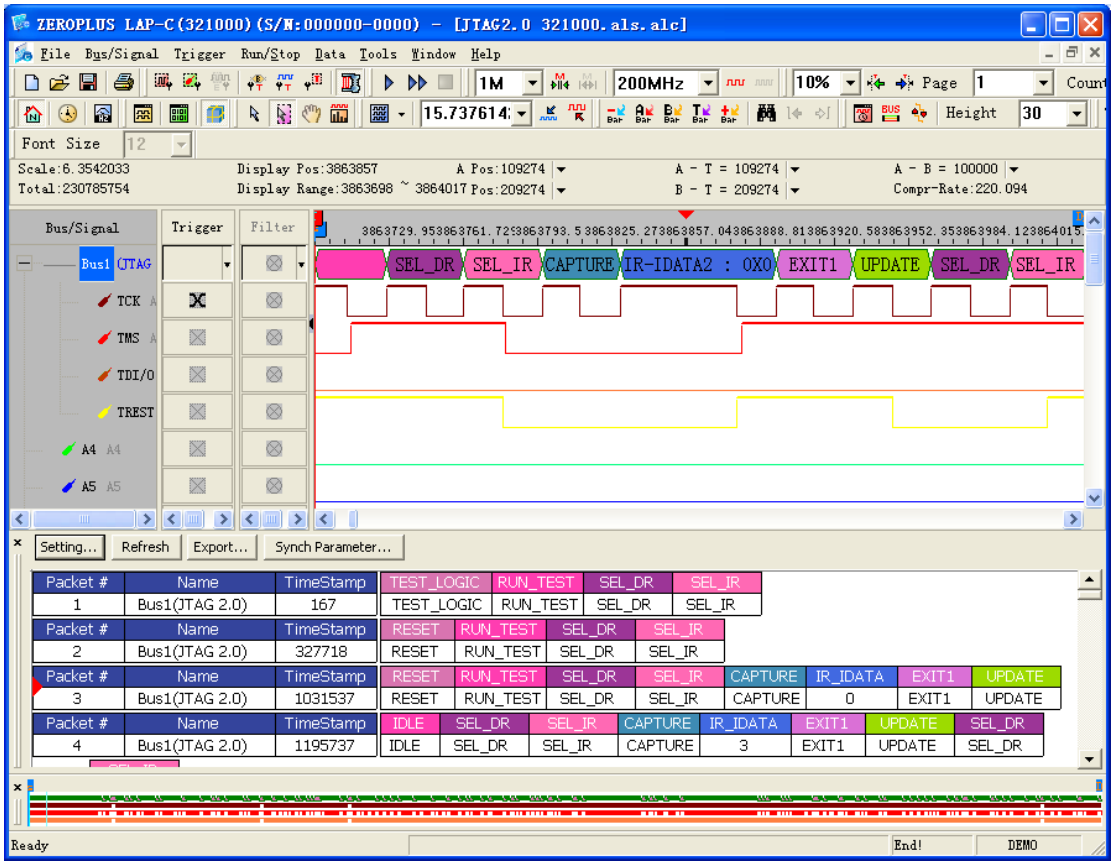
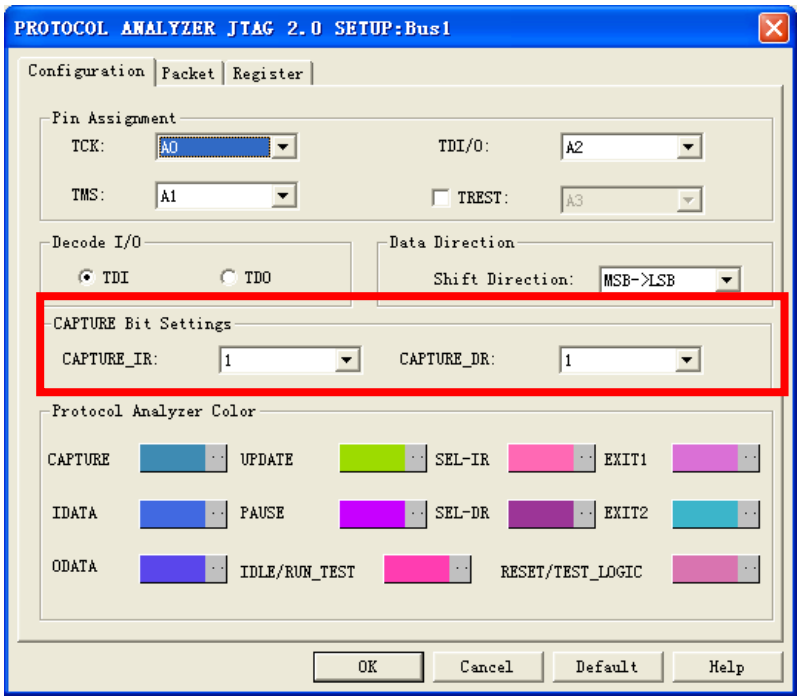


Figure 8: Captured JTAG Signals

The Protocol Analyzer JTAG of the Zeroplus Technology Logic Analyzer not only can analyze the packet of the signal automatically, but also can set the bit length for the CAPTURE_IR and CAPTURE_DR depending on the content of the signal. The configuration interface is shown as the *Figure 9*.

中和市建八路 123 號 2F
電話：886-2-66202225
傳真：886-2-22234362
www.zeroplus.com.tw

2F., No.123,Jian Ba Rd,
Chung Ho City, Taipei Hsien, R.O.C.
Tel: 886-2-66202225
Fax: 886-2-22234362



Set the bit length for the CAPRURE_ID and the CAPTURE_DR

Figure 9: Configuration Interface of the Protocol Analyzer JTAG of Zeroplus Technology Logic Analyzer

中和市建八路 123 號 2F
電話：886-2-66202225
傳真：886-2-22234362
www.zeroplus.com.tw
2F., No.123,Jian Ba Rd,
Chung Ho City, Taipei Hsien, R.O.C.
Tel: 886-2-66202225
Fax: 886-2-22234362

Conclusion:

The JTAG interface not only can be used to test the device, but also can be used to compile the different devices. At present, many new-arrival microprocessors support the JTAG interface; even the Protocol Analyzer PCI supplies the pins for the JTAG signal. Furthermore, the JTAG interface can be made to be the debugging system with the Probe Mode, which is a kind of powerful system debugging mode. And a microprocessor which is connected to the test controller through the JTAG can be used as an ICE (In – Circuit Emulator), which is very convenient for the R&D engineers.

Zeroplus Technology Logic Analyzer has released more than 56 kinds of Protocol Analyzers. When engineers analyze the signal of the Protocol Analyzer, they can use the automatic decoding function of the software to reduce the time of developing the project, and make the product on the market earlier. At the same time, when they analyze the different kinds of digital signals, it is unnecessary to decode the signal to be tested in the mode of manual decoding. If you want to learn more information of our Zeroplus Logic Analyzer, please visit the Zeroplus Technology Website, www.zeroplus.com.tw.

References

Michael Gook (editor), Chen Liguang (translator). Completely Research of the PC Hardware Interface. Flag Press.

Liao Yuping, Lu Ruiqiang. Design of the System Clip -- Use Quartus II.