Debugging UART Buses in Embedded System Designs

UART (Universal Asynchronous Receiver-Transmitter)
UART stands for universal asynchronous receiver and transmitter; pronounced “you-art.”, is for any serial port communication. The UART is framing the data byte by setting “Data bits”, “Parity bits”, “Stop and start bits”, “Baud Rate” and “LSB or MSB”.

UART Sampling Received Data

UART Data Bits Frame
Start Bit: a bit indicates the start of a byte.
Data Bits: numbers of data bits are used in a frame. Eight bits of data is the most common.
Parity bit:
check the even or add numbers of 1 are received. (Even = true when even number of 1s)
Stop bit: a bit indicates the stop of a byte.
Baud: sampling bits per second. (9600 is usually applied on serial terminals)
LSB: data bits started from left to right direction.
MSB: data bits started from right to left direction.

RS-232
RS-232 is defined in early 1960, the well know data byte frame of UART. It is widely used in PC serial ports and embedded systems for serial communication between two devices over a short distance.

RS-232 Connectors
The RS-232 connectors have got two models, 9 pins and 25 pins as the figure below:

9-Pin D-sub (DE-9, often called DB-9)

25-Pin D-sub (DB-25)

RS232 Signals & DTE-to-DCE DB-9 connection (Straight cable)
**Debugging RS-232 Buses By Using Oscilloscope vs. Zeroplus PC based Logic Analyzer**

**Example:**
Measure an RS-232 Bus was generate from 8051 micro control

**Signal stats:**
- Baud rate: 9600 bps
- Data bit: 8 bit
- Stop bit: 1 bit
- Parity Check: Yes

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**Debugging UART Bus by Using Oscilloscope**

1st Step:

- Setup conditions of oscilloscope to catch UART signal.
- Trigger level: CH2 ring edge.
- Frequency: <10Hz
- Operating time consumed: 10~15 seconds.

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**Debugging UART Bus by Using Zeroplus PC Based Logic Analyzer**

1st Step:

- Set trigger condition as below: A0: rising edge
- Operating time consumed: about 8 seconds.
Enlarge screen, and the data can’t be recognized.
Setup frequency to re-sampling.
Operating time consumed: about 5 seconds.

Set up UART Bus self-definitions.
Parity: none parity,
Data Bit = 8
Data Direction = MSB -> LSB
Baud Rate = 9600
Stop bit = 1
Sample Rate = 70%
Operating time consumed: 2~5 seconds.

Enlarge UART signals caught to view and analysis the signals clearly and easily.
Operating time consumed: 20~30 seconds.

Re-set up oscilloscope at right sampling to catch UART signal.
Decoding UART signal manually.
Operating time consumed: 8~10 minutes are consumed to decode an Address & 8 bits data.
Transfer parallel buses into serial buses are widely applied in embedded systems design, but it is difficult to be diagnosed problems by using traditional oscilloscopes. Zeroplus LAP-A series PC based logic analyzers provide the economical solution with powerful trigger, decode and search capabilities to design engineers solving embedded system design issues with exceptional efficiency.

Conclusion
Transfer parallel buses into serial buses are widely applied in embedded systems design, but it is difficult to be diagnosed problems by using traditional oscilloscopes. Zeroplus LAP-A series PC based logic analyzers provide the economical solution with powerful trigger, decode and search capabilities to design engineers solving embedded system design issues with exceptional efficiency.