



## LAP-A Specification

Model		LAP-16128U	LAP-32128U-A	LAP-321000U-A
<b>Operating System</b>		Windows	Windows	Windows
		98SE/ME/2000/XP	98SE/ME/2000/XP	98SE/ME/2000/XP
<b>Interface</b>		USB2.0	USB2.0	USB2.0
<b>Power</b>	Power	USB	USB	USB
	Power Dissipation (running)	1W	1W	1W
	Power Dissipation (startup)	2W	2W	2W
<b>Sample rate</b>	Internal clock (Timing Mode)	100HZ~200MHZ	100HZ~200MHZ	100HZ~200MHZ
	External Clock (State Mode)	100MHz	100MHz	100MHz
	Bandwidth	75MHz	75MHz	75MHz
<b>Memory</b>	Memory	4Mbits	4Mbits	32Mbits
	Depth (per channel)	128Kbits (Max 32Mbits for Compression)	128Kbits (Max 32Mbits for Compression)	1Mbits (Max 255Mbits for Compression)
<b>Trigger</b>	Condition	Pattern/Edge	Pattern/Edge	Pattern/Edge
	Trigger channel	16CH	32CH	32CH
	Pre/Post Trigger	YES	YES	YES
	Waveform Trigger Width	NO	NO	NO
	Trigger Level	One Level	One Level	One Level
	Trigger Count	1~65535	1~65535	1~65535
<b>Threshold Voltages</b>	Working range	-6V ~ +6V	-6V ~ +6V	-6V ~ +6V
	Accuracy	±93mV	±93mV	±93mV
<b>Maximum Input Voltage</b>		±30V	±30V	±30V
<b>Impedance</b>		500KΩ/10pF	500KΩ/10pF	500KΩ/10pF
<b>Bus / Protocol</b>	I <sup>2</sup> C / UART	Free	Free	Free
	SPI	Option	Free	Free
	1-WIRE / HDQ / CAN BUS	Option	Option	Free
	SIGNIA / I <sup>2</sup> S / SSI / Microwire	Option	Option	Option
	PS/2 / USB1.1/ Manchester	Option	Option	Option
	S/PDIF / Lin BUS	Option	Option	Option
<b>Data Skew</b>		<1.5ns	<1.5ns	<1.5ns
<b>Certification</b>		FCC/CE/BSMI/WEEE/RoHS	FCC/CE/BSMI/RoHS	FCC/CE/BSMI/RoHS
<b>Package Contents</b>				
Analyzer (130mm x 100mm x 30mm / 175g)		1	1	1
USB cable		1	1	1
16/32 channel testing cable package (25cm)		1 Pack 8pin*2 / 2pins*1/ 1pin*1	1 Pack 16pins*1 / 8pin*2 / 2pins*1/ 1pin*1	1 Pack 16pins*1 / 8pin*2 / 2pins*1/ 1pin*1
Probes (test grabbers)		1 Pack 20 pieces/Package	1 Pack 36 pieces/Package	1 Pack 36 pieces/Package
Software / Documentation CD		1	1	1
Installation Guide		1	1	1



### Recommended Tool Bag



### Features

- SPI, I<sup>2</sup>C, UART, 1-WIRE, HDQ, CAN BUS, USB1.1, SIGNIA RF MODULE, I<sup>2</sup>S, PS/2, Microwire, SSI, Manchester ...bus communication protocol analysis allows you to easily develop circuits interfacing as the protocols mentioned.
- Supports time stamps, bus values, binary, hex, ASCII, decimal, etc display with timing wave.
- **Memory per Channel**
  - 128KB (or 1MB\*) per channel without compression.
  - Hardware compression ratio up to 255:1 depending on activity.
  - Analyze more data at one time and simplify your debugging task.
- **Flexible Sampling Frequency for accuracy**
  - Synchronous operation (use test-board clock) : Max 100MHz
  - Asynchronous operation (use logic analyser clock) : 100Hz ~ 200MHz
- **Hook up with benchtop tools e.g. Oscilloscope, etc.**

Equipped with output pins to synchronize logic analyzer operations with other benchtop analysis tools.

  - Read Out pin
  - Trigger Out pin
  - Start Out pin



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