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Cheng

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(54) **METHOD FOR DATA ACCESSING AND MEMORY WRITING FOR LOGIC ANALYZER**

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See application file for complete search history.

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(56) **References Cited**

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U.S. PATENT DOCUMENTS

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4,550,387	A *	10/1985	Takita	377/55
4,558,422	A *	12/1985	DenBeste et al.	702/57
5,144,225	A *	9/1992	Talbot et al.	324/73.1
5,608,866	A *	3/1997	Horikawa	714/39
5,933,594	A *	8/1999	La Joie et al.	714/26
2002/0159086	A1 *	10/2002	Shinomiya et al.	358/1.13
2006/0143518	A1 *	6/2006	Cheng et al.	714/25
2007/0047458	A1 *	3/2007	Adkisson	370/252
2007/0220352	A1 *	9/2007	Hernandez et al.	714/39
2008/0240370	A1 *	10/2008	Wang et al.	379/30
2008/0301500	A1 *	12/2008	Genden et al.	714/30
2010/0027031	A1 *	2/2010	Stimpson et al.	356/614
2010/0223502	A1 *	9/2010	Brunot et al.	714/29

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* cited by examiner

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(57) **ABSTRACT**

A method of fetching digital data and writing the digital data into a memory of a logic analyzer, which comprises the steps: designate at least a first region and a second region in a memory; set a first triggering condition and a second triggering condition; fetch digital data continuously and write it into the memory while analyzing; and then write first test data which have an identification to satisfy the first triggering condition into the first region, and write second test data which have an identification to satisfy the second triggering condition into the second region. And once the first test data or the second test data are found, stop writing the digital data into the corresponding regions.

17 Claims, 3 Drawing Sheets

