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LAP-B Logic Analyzer Powerful Upgrading !







Ultra High Timing Sample Rate: Up to 2G Hz

Hire double timing sample rate than original series to "2GHz". Higher measure capacity and resolution to capture DUT signal more precisely!



4 Giga Data Compression Rate !

No more upset over debug problem that caused by insufficient memory depth~ Powerful patented function—"Data Compression" up to 2^32 times under each high speed capture mode, maximize the memory resource.



Flexible allocation of channel/memory !

When measuring serial bus signal you usually don't need too many channels. The new LAP-B(702000R) provides the "MEMOFOLD Mode" that allocate memory to each channel. Sophisticated & no idle resource!

Channel	64 ch	32 ch	16 ch	8 ch	4 ch	2 ch	1 ch
Depth	2M bits	4M bits	8M bits	16M bits	32M bits	64M bits	128M bits



Hardware Upgrade : 256 Multi-Level Trigger

More trigger level let more configurable condition to capture troublesome bug. LAP-B(702000R) hire 256 Multi-Level Trigger that provide you powerful debug capacity !



Serial Bus Protocol Hardware Trigger

The new LAP-B(702000R) provide "real-time" hardware protocol trigger, precisely trigger by specific protocol packet condition once it occurs on the circuit. So far it support serial protocols including: I²C 、 SPI 、 UART 、 CAN BUS & SVID.

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